COLD DELAY DEFECT SCREENING

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Abstract

Delay defects can escape detection during the normal production test flow, particularly if they do not affect any of the long paths included in the test flow. Some defect types can have their delay increased, making them easier to detect, by carrying out the test with a very low supply voltage (VLV testing). However, VLV testing is not effective for some delay defects such as high resistance interconnnects. This paper presents a screening technique for such defects. This technique relies on carrying out the test at low temperature. One particular type of defect, salicide resistive opens, is analyzed and experimental data is presented to demonstrate the effectiveness of cold testing.

1. Introduction

Timing failures occur when the delay of the manufactured circuits is different from the designed delay. A circuit has a *delay fault* if there is a timing failure that makes the circuit fail to work at the designed speed but to be functional at a slower speed [Franco 91, Lesser 80, Shedletsky 78, Smith 85]. As of today, most studies on testing timing failures concentrate on the detection of delay faults *i.e.* delay fault testing [Lin 87, Natarajan 99, Krstie 99, Tragoudas 99]. Although timing failures may be detected by delay fault testing, the success of detection really depends on the significance of the excess delays caused by timing failures. For example, some timing failures that are embedded in short paths may not cause delay faults at normal operating conditions, thus they are not detectable by delay fault testing.

Chang and McCluskey showed that very-low-voltage testing *(VLV testing)* can enhance the magnitude of the excess delays caused by *delay defects* and thus improve their detectability [Chang 96]. Table 1 lists the causes of delay defects and the corresponding effectiveness of VLV testing on them [Chang 98]. As listed in table 1, VLV testing is effective in detecting most delay defects except *high resistance interconnects*. High resistance interconnect can happen at global interconnect (metals), local interconnect (polysilicons), and vias to increase their resistance. In a future technology, signal can propagate through many polysilicons, vias, and metal layers before reaching the receiving ends; variations of the resistance in the signal path can have a significant impact on the timing of the path. Therefore, it is necessary to find cost-effective ways to detect high resistance delay defects to eliminate the potential timing failures.

Table 1: Causes of delay defects and effectiveness of VLV testing [Chang 98]

Causes at transistor level	Detected by VLV
Transmission gate opens	Yes
Threshold voltage shifts	Yes
Diminished-drive gates	Yes
Gate oxide shorts	Yes
Metal shorts	Yes
Defective interconnect buffers	Yes
High resistance interconnects (via, polysilicon, metal)	*No*

In this paper, we report a *low temperature screening* technique to screen out *salicide resistive open defects*, a common cause of high resistance interconnects. In today's technology, a salicide thin film is deposited on top of the polysilicon as a shunt layer to reduce the effective resistance of the polysilicon. At a lower temperature, the resistance of the polysilicon with salicide resistive opens increases. Therefore, salicide resistive opens are more detectable at low temperature because the excess delay caused by salicide resistive opens become more significant. Experimental results will be presented to validate the effectiveness of the low temperature screening technique. The selection of test speed, test voltage and the target parameters to test for the low temperature screening techniques will also be discussed.

Our techniques can actually be extended to improve the detectability of the defects that can be accelerated by low temperature, *i.e.* the *cold defects* [Needham 98]. Cold defects escape all tests at normal temperature but can be detected at low temperature. In our experiment, cold defects other than salicide resistive opens have been located as well. According to the experimental results, they cause either catastrophic failures or timing failures. As of today, we are still investigating their failure mechanisms and the corresponding fault models. In this paper, we will only focus on salicide resistive opens due to the completeness of data.

This paper is organized in the following way. Section 2 describes the failure mechanism of salicide resistive open

and explains how its resistance changes with temperatures. Section 3 describes the experiment setup. Section 4 presents the experiment results of experiments are presented and discussed in section 4. Section 5 concludes the paper.

2. Silicide Opens

2.1 Polysilicon and Silicide

Polycrystalline silicon (polysilicon) is used for both the gate electrodes and local interconnects in CMOS technology. Its good thermal stability, good interface to silicon dioxide, good conformality and ease of deposition and processing has made it a mainstay of silicon technology. However, as the circuits got faster, the sheet resistivity of polysilicon starts to limit the overall speed of the circuits. For a 0.5um thick polysilicon, the sheet resistance is about 10 Ohms/square compared to 0.05 Ohm/square for Al of the same thickness [Plummer 98]. To reduce this problem, *silicide* is used in shunt with polysilicon to reduce the equivalent resistance.

Silicide is formed by depositing the metal onto the polysilicon. The wafer is then annealed at high temperature and the silicide forming reaction occurs wherever the polysilicon and metal are in contact. There have been several silicide materials used in silicon technology, including WSi2, TaSi2, TiSi2 and CoSi2. Among the materials, TiSi2 is the most popular due to its ability to adhere well to most other materials and its low resistivity. Typical sheet resistance of TiSi2 is about 1.2 Ohm/square, which is about ten times less than that of polysilicon. The equivalence resistance of a polysilicon with silicide is thus about 10 times lower than that of a polysilicon.

2.2 $TiSi_2$ Failure Mechanism

$TiSi_2$ is formed by depositing Ti over the polysilicon, followed by a two-step anneal. The first anneal is at low temperature, about 600^{o}C for about 15-60 seconds. Any unreacted Ti is then selectively etched off. After the first anneal, $TiSi_2$ is in a metastable, "C49", phase, which has a higher resistivity of 60-70 uOhm-cm. A 800^{o}C second anneal for about 30-60 seconds is required to transform TiSi2 to the equilibrum, "C54", phase, which has a lower resistivity of 13-20 uOhm-cm [Plummer 98].

The higher temperature and longer time for the second anneal can lead to *agglomeration* inside the silicide. If agglomeration occurs, the grain boundaries in the silicide may be wide open such that the silicide becomes totally or only partially connected. As a result, an *open defect* exists on the line composed of polysilicon and silicide. Figure 1 shows a TEM image of a silicide open.

The occurance of agglomeration also depends on the dimension of the silicide. The anneal time is proportional to the size of the silicide and is usually decided by the time needed to transform the largest silicide on the wafer from the C49 phase to the C54 phase. However, the time might be too long for the smaller silicides on the same wafer. As a result, opens might occur on the smaller silicide because of agglomeration. This also indicates that silicide open defects, which are caused by agglomeration, will become a more serious problem in sub-micron technologies due to the decreasing minimum feature size.

In summary, aglomeration is the major failure mechanism of silicide open. It is a process-induced failure mechanism and will become more severe in deep-submicron technology due to the smaller dimesions, even with well-controlled anneal time and temperature. In [Needham 98], the authors reported silicide open as a major cause of reliability fallouts and constitutes 60dpm of the defect level. The data from Intel also show that the failures can be seen at low temperature, would be marginal at room temperature, and would pass at high temperature. Therefore, silicide open is a *real* defect and needed to be screened out during production testing.

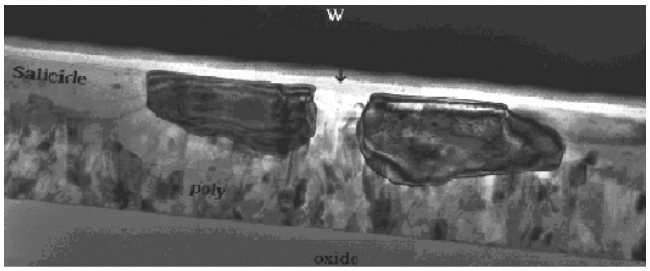

Figure 1: TEM image of $TiSi_2$ open defect over polysilicon.

2.3 Temperature Coefficient of Defect Resistance

Figure 2(a) illustrates the current path in a local wire, which consists of a normal silicide on top of a polysilicon line. Most currents flow inside the silicide due to its much lower sheet resistance, $R_{S,G}$. The equivalent resistance, R_{eq}, is dominated by $R_{S,G}$.

As temperature decreases, the resistance of silicide also decreases due to less lattice vibrations [Nava 93]. Because R_{eq} is dominated by $R_{S,G}$, R_{eq} will also decreases as temperature decreases, i.e. the temperature coefficient of the equivalence resistance is positive. Any circuit that is free of silicide open defects should operate faster at lower temperature, because the delay associated with the local wire is smaller at lower temperature.

When there is a salicide resistive open, as depicted in Figure 2(c), the low resistance shunt path over polysilicon is partially or totally broken. In this case, the current will split into two paths, as depicted in Figure 2(d). One current path still flows through salicide, but with a resistance $R_{S,D}$, which is greater than $R_{S,G}$ due to smaller cross-section area of salicide. The other current path originates from salicide to the polysilicon layer, then flow back to the salicide on the other side of the opening. The resistances in the second current path, $R_{P,}$ include the resistances on the two salicide/poly-Si interfaces, R_{int1} and

R_{int2}, and the resistance in the polysilicon layer, R_{poly}. Therefore, the total resistance in the second current path is:

$$R_P = R_{poly} + R_{int1} + R_{int2}. \quad (1)$$

and the equivalent resistance R_{eq} is:

$$R_T = \frac{R_P R_{S,D}}{R_P + R_{S,D}} = \frac{R_p}{\frac{R_p}{R_{S,D}} + 1} \quad (2)$$

The resistance of polysilicon has a negative temperature coefficient, that is, its resistance increases as the temperature decreases [Kamins 88]. In addition, the electrons will need to overcome two Schottky barriers at the interfaces between polysilicon and silicide. The equivalent resistance of the Schottky junctions also increases as temperature decreases [Kamin 88]. Therefore, the total resistance of the current path inside polysilicon, R_P, will also increases as temperature decreases. Following the simple RC delay model, we conclude that the delay increases as temperature decreases.

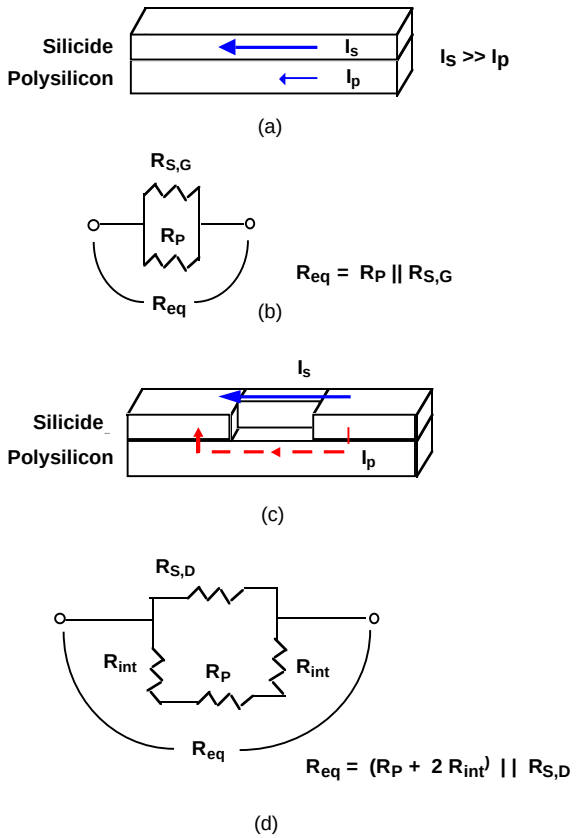

Figure 2: (a) Current path in a wire consisting of defect-free silicide on top of polysilicon; (b) The equivalent circuit for (a); (c) Current paths in a wire consisting of silicide open on top of polysilicon; (d) The equivalent circuit for (d)

In conclusion, silicide open defect can be accelerated in a low temperature environment. At low temperature, the resistance of a silicide open defect increases due to its negative temperature coefficient. Therefore, a silicide open defect is more likely to be detected because the delay corresponding to the open defect becomes larger.

3. Experiment

An experiment has been performed at Intel to validate the low temperature screening technique. The circuit-under-test (CUT) is a microprocessor. The nominal operating voltage for the CUT is 1.6V and the nominal operating frequency is 333 MHz.

3.1 *minVCC* Test

Two performance parameters are commonly used to decide if there is any delay fault inside a CUT: *maximum operation frequency* (*Fmax)* and *minimum operation supply voltage (minVcc)*. *Fmax* is the maximum clock frequency that the CUT can still function correctly for all the test patterns, at some specified supply voltage. *Fmax* testing is basically a Shmoo testing, in which the *Fmax* value corresponding to various supply voltages are recorded. However, the ability to implement *Fmax* testing is limited by the power and the speed the tester can provide. As circuits speed increases, it will be very expensive to implement *Fmax* testing.

The speed of a circuit is dependent on the supply voltage [Wagner 85]. At a supply voltage lower than the nominal value, the circuits' switching speed will be lower than that at the nominal supply voltage. When the supply voltage is too low, the circuit will stop functioning at all for all test patterns. The maximum supply voltage where the CUT fails completely is called *minVcc* [Ager 82]. Although it is only an indirect indication of the chip speed, it is more cost-effective than *Fmax* testing due to the lower power and lower speed required from the tester.

3.2 Experimental Flow

Figure 3 shows the experiment flow. After manufacturing, all CUTs were tested at wafer levels at 0°C. We then performed two *minVcc* tests on randomly selected CUTs that passed wafer tests. The first *minVcc* test was applied at the frequency of 333 MHz, while the second *minVcc* test was applied at the frequency of 100MHz. The selection of CUTs in the two *minVcc* tests are independent As a result, some CUTs were tested at both frequencies, some CUTS were tested at either frequency, and some CUTs were never tested. The results from the two *minVcc* tests are not used to reject any CUT.

All CUTs that passed wafer tests were packaged and tested functionally at 100°C. Eighteen thousand, nine hundred and sixty-five packaged CUTs, which were selected randomly from all CUTs that passed the tests at 100°C, were tested at 0°C again. There are 53 CUTs that

failed the tests at 0°C and they are classified as the *cold rejects*.

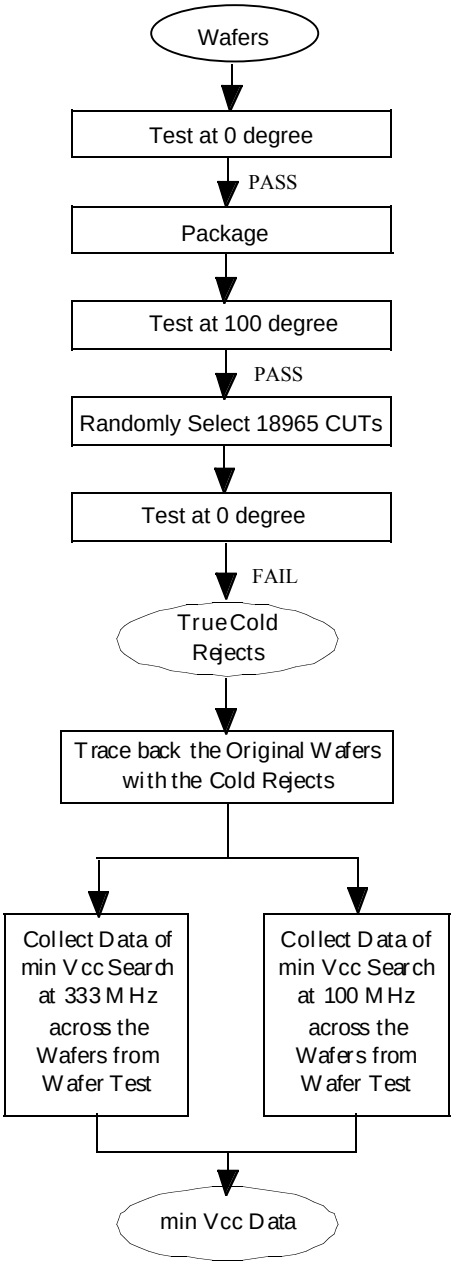

Figure 3: Test Flow

The wafers that contain these 53 cold rejects are identified using the data from the two *minVcc* tests at wafer level. The *minVcc* test results of the CUTs on these wafers, including both good CUTs and cold rejects, were analyzed to decide the effectiveness of low temperature test at wafer level. Figure 4 shows the breakdown of the 53 cold rejected CUTs: 24 CUTs were tested by the 333 MHz *minVcc* test, 13 were tested by the 100 MHz *minVcc* test, and 9 CUTs were tested by minVcc tests at both frequencies.

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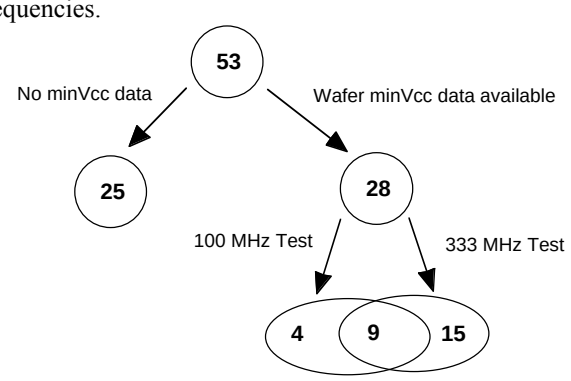

3.3 Results

Figure 4 shows the cumulative distribution of CUT minVcc values for 7 wafers. The results are from the 333MHz test. All 7 wafers consist of good CUTs and cold rejects. Each line in the figure represents a set of CUT minVcc values for the same wafer. The hollow marks show the minVcc values of good CUTs, while the solid marks show the minVcc values of the cold rejected CUTs on the corresponding wafer.

At the same supply voltage, a cold reject operates at a slower speed than a good CUT due to the longer delay cause by cold delay defects. That is to say, a cold reject needs higher supply voltage to achieve the same speed than a good CUT. As shown in Figure 4. a cold reject has higher minVcc than good CUTs on the same wafer.

The minVcc distribution also shows that there is a gap of minVcc values between cold rejects and good CUTs. This is true for all seven wafers. The minimum gap size is about 0.1V, which is significant with respect to the normal supply voltage of 1.6V. This indicates that the excess delay caused by salicide opens becomes significant at low temperature. By properly setting a threshold of minVcc

value in the gap, most cold rejected CUTs can be separated from the good CUTs effectively.

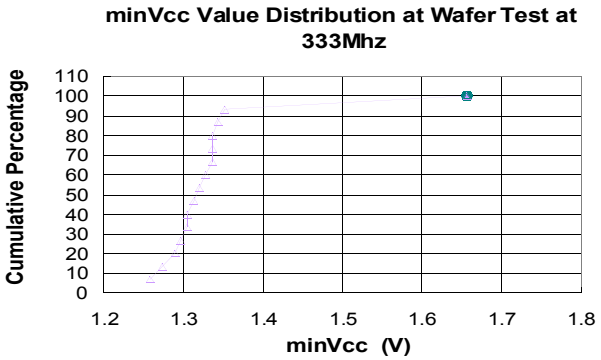

Figure 4: Cumulative distribution of minVcc at 333 MHz wafer test

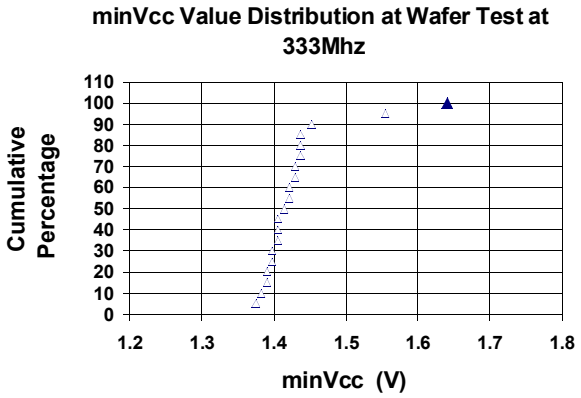

Table 4 compares the effectiveness between the 100MHz test and the 333 MHz test. The sample size is nine, which is the number of cold rejects that have been tested at both 100 MHz and 333 MHz for their minVcc value. The results show that the 333 MHz detects all nine cold rejects but the 100MHz test only detects seven out of nine.

Table 4: Effectiveness of minVcc test at different frequency

Test Frequency	Detected by wafer minVcc test	%
100 MHz	7	77%
333 MHz	9	100%

Figure 5 shows the comparison of minVcc distribution for a wafer tested at both 100 MHz and 333 MHz. It shows that at the higher test frequency, the minVcc has a higher value and wider distribution than at the lower test frequency. Moreover, minVcc value of the cold rejected CUT is mixed with those of good CUTs at the 100MHz test, while the minVcc value of the cold rejected CUT is at the tail of the distribution at the 333 MHz test. The results indicate that the screening is more effective running at 333MHz.

The delay of an IC is smaller at low temperature [Glasser 85]. thus the IC needs to be tested at high frequency to screen out the timing failures. Our result indicates the same scenario. The narrow distribution of minVcc values of the 100MHz test shows that there is too much time slack reserved for the paths including the salicide opens at the 100MHz test. The delay of a cold reject is not much different from a good CUT in this condition. Thus the 100MHz test has more escapes than the 333 MHz test.

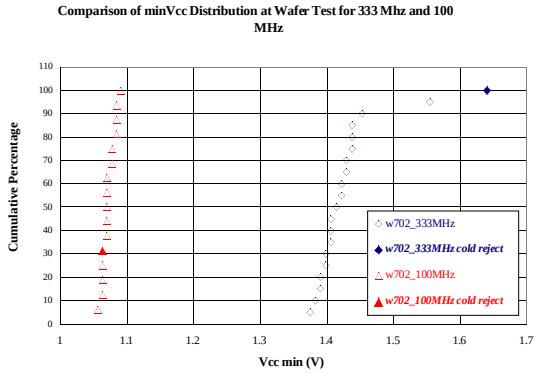

Figure 5: Comparison of cumulative distribution of minVcc at wafer test at 100 MHz and 333 MHz

5. Conclusions

In this paper, We presented a low temperature screening technique that detects cold delay defects such as salicide resistive open. The effectiveness of this technique is validated by wafer test results of a microprocessor. The equivalent circuit of a defect-free and a salicide resistive open defect were analyzed. When a salicide resistive open defect occur, the current is forced to flow through the polysilicon, that has higher resistance and reversed temperature coefficient. Therefore, the speed of circuit becomes slower. When the resistance in the defective salicide path is much larger than the resistance in the salicide-polysilicon-salicide path, the speed of circuit will become even slower at low temperatures. Therefore, the delay defect is easier to be detected at low temperatures.

The selection of test speed and the target parameters to test for the low temperature screening techniques have also been discussed. Experiment results show that 83% of the cold delay defects have been screened out by correctly setting threshold minVcc value in tests at high speed, which may not necessarily be the specified operating speed. Our techniques can actually be extended to detect a more general class of delay defects with such temperature-sensitive property.

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