# An Evaluation of Pseudo Random Testing for Detecting Real Defects

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## Abstract

*Research has shown that single stuck-at fault (SSF) N-detect test sets are effective for detecting defects not modeled by the SSF model. Experimental results showed N-detect coverage is a good metric for determining test quality. In this paper, we examine the test quality of pseudo-random Built-In-Self-Test (BIST) patterns by quantifying the relations between their N-detect coverage and test length. We theoretically derive bounds on the minimum test length of pseudo-random patterns required to achieve a given N-detect coverage. For faults with high detectability, the expected test length for N-detection is around N times the expected test length for single detection. However, for faults with low detectability, the expected test length for N-detection can be NlogN times the expected test length for detecting the fault only once; this increases the test length significantly. We also introduce the idea of effective detectability which is important for analyzing the effectiveness of BIST techniques for detecting real defects.*

## 1. Introduction

Built-in Self Test (BIST) allows an integrated circuit (IC) to test itself [McCluskey 85]. By embedding the test pattern generators, an IC can be tested at-speed to reduce the test time. In addition, timing-related defects and unmodeled defects are more likely to be detected. By embedding the output response analyzers, BIST eliminates the need for expensive test equipment to capture the output responses precisely and rapidly. Moreover, BIST can be used for testing the IC in the field.

Most BIST architectures use pseudo-random test pattern generators, such as linear feedback shift registers (LFSR), to perform test pattern generation. The quality of pseudo-random patterns is evaluated by calculating their stuck-at fault coverage. The relationship between the expected fault coverage and test length for psuedo-random patterns has been derived in [McCluskey 88]. Defect-based testing is an emerging paradigm in VLSI test in which real production defects are targeted and test techniques are developed to detect these defects (rather than faults). For more details of the defect-based testing paradigm, the reader is referred to the lecture series in the proceedings of the International Test Conference, 2000 [ITC 00]. However, very surprisingly, there is no publication which quantifies the effectiveness of BIST patterns in detecting real defects. Almost all commercial tools and publications report the single stuck-at fault coverage to quantify the effectiveness of BIST patterns. In this paper, we address the problem of quantifying the defect coverage of pseudo-random BIST patterns.

Although the single stuck-at fault model is a widely used fault model, it is not accurate and does not model the behavior of production defects very well [McCluskey 00]. Test vectors generated using the stuck-at fault model do not necessarily guarantee the detection of all defective parts. In order to increase the defect coverage of the single stuck-at fault test vectors, *N*-detect single stuck-at fault test vectors were considered. In an *N*-detect single stuck-at fault test set, each single stuck-at fault is detected by different test vectors at least *N* times, or the maximum number of times the fault can be detected. By detecting each stuck-at fault many times, the chance that other unmodeled defects (often called surrogates) are detected increases significantly [Pomeranz 98]. In the Murphy test chip experiment, all the 116 defective chips were detected by single stuck-at test sets that detect each single stuck-at fault 3 or more times; however, the best 100% stuck-at test set missed 2 defective chips [Ma 95]. It was later observed that all N-detect test sets have higher transition fault coverage than other 100% SSF test sets. In [Grimaila 99], it was reported that the defect level was improved by 1288dpm, after applying *N*-detect single stuck-at test sets. Therefore, *N*-detect single stuck-at fault coverage is a better metric for defect coverage compared to the traditional stuck-at fault coverage.

In this paper, we examine the test quality of pseudo-random test patterns using the *N*-detect coverage as the metric. We derive theoretically the bound on the expected length of pseudo-random test patterns for detecting a stuck-at fault *N* times by different test vectors. We also present simulation results for several circuits. Our theoretical bounds and simulation results show that pseudo-random test patterns can achieve good *N*-detect coverage; however, under certain circumstances the test length can be very large. For detecting a single stuck-at fault *N* times, the expected test length may be between *N* and *N*log*N* times the expected test length for detecting the fault only once. For example, to detect a fault 20 times, the test length can increase to approximately 30 times the test length required to detect the fault only once.

As part of our analysis technique, we introduce the concept of effective detectability of a single stuck-at fault. This concept is extremely important while grading BIST patterns to quantify their defect coverage.

This paper is organized as follows. Section 2 briefly describes why *N*-detect stuck-at test sets are effective for detecting real defects. In Sec. 3, we derive the theoretical bound on the expected length of pseudo-random test patterns required for detecting a given single stuck-at fault *N* different times. We also introduce the idea of effective detectability and discuss the implications of our results for BIST architectures and techniques in Sec. 3. Section 4 presents simulation results for several circuits. Section 5 concludes this paper.

## 2. Stuck-at Fault *N*-detect Tests

Figure 1 illustrates why single stuck-at fault *N*-detect tests are effective in detecting defects that can not be modeled by as stuck-at faults. There are three input patterns that can detect the fault Z/1: (WXY) = (001, 011, 101). Any test set with 100% SSF coverage needs to include only one of these three patterns.

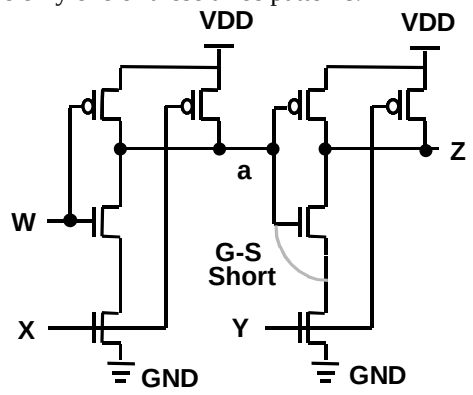


Figure 1. Circuit to illustrate N-detect test sets.

Suppose that a defect causes a resistive gate-to-source short (G-S short) in an NMOS transistor as shown in Fig.1. For certain values of the resistance of the short, this G-S short can be detected only by the patterns (WXY) = (011) or (WXY) = (101). A 100% SSF test set will not detect the G-S short if it only consists of the pattern (WXY) = (001). However, in a test set in which each SSF must be detected at least three times, (also called a *3-detect single stuck-at fault* test set or SSF 3-detect test set), all three of these patterns must be included. Therefore, a SSF 3-detect test set is more likely to detect the G-S short of Fig. 1 compared to a 100% SSF test set, even though the G-S short can not accurately modeled as a SSF fault.

Table 1. Effectiveness of SSF test in detecting G-S short

| W | X | Y | Z | Z/1 | G-S short |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | detect | **escape** |
| 0 | 1 | 1 | 1 | detect | detect |
| 1 | 0 | 1 | 1 | detect | detect |

## 3. Expected Length of *N*-detect Test Patterns for Pseudo-Random BIST

In this section, we derive upper and lower bounds on the expected test length of pseudo-random patterns for detecting a given single stuck-at fault *N* times by different test patterns. To model a realistic BIST environment, we assume that the number of vectors applied is much less than the number of all possible input combinations that can be obtained from the LFSR. This assumption is realistic and justified [McCluskey 88]. As explained in [McCluskey 88], this assumption allows us to treat the BIST test patterns as random patterns although they are actually pseudo-random. In Appendix A, we derive the expected test length of pseudo random patterns for detecting a fault N times without these assumptions.

Suppose that we have an *m*-input combinational logic circuit C. Let $M$ (= $2^m$) be the total number of all input combinations that can be applied to this combinational logic circuit C. Consider a single stuck-at fault *f* in *C*. Let us suppose that the *detectability of the fault f* is *k, i.e., k* is the total number of input combinations that detect the fault *f*. We apply random patterns at the inputs of *C* and try to detect *f* by *N* different input combinations, where $N \le k$.

The expected number of random patterns that we must apply to detect the fault *f* once is equal to $\frac{M}{k}$. This is because, the probability that the fault *f* will be detected by the first pattern is $\frac{k}{M}$; the probability that it will detected by the second pattern is $(1-\frac{k}{M})\frac{k}{M}$, and so on. Hence, the expected test length is $\frac{k}{M} + 2(1-\frac{k}{M})\frac{k}{M} + 3(1-\frac{k}{M})^2\frac{k}{M} + .... = \frac{M}{k}$.

Let $g(N)$ be a random variable which represents the test length to detect *f* using *N* different random patterns. $E[g(N)]$ is the expected value of $g(N)$. We can write the following recurrence relation:

$$E[g(N)] = E[g(N-1)] + p_N + 2(1-p_N)p_N + 3(1-p_N)^2 p_N + ....,$$

where $p_N = \frac{k-N+1}{M}$.

Intuitively, the above recurrence relation is true because, for detecting a fault using *N* different test patterns, we must first detect it with *N*-1 different test patterns; for the *N*th detection, none of the previous *N*-1 test patterns can be used. The above recurrence relation can be solved as follows:

$E[g(N)] = E[g(N-1)] + \frac{1}{p_N}$. This is because,

$$p_N + 2(1-p_N)p_N + 3(1-p_N)^2 p_N + .... = \frac{1}{p_N}$$

Therefore,

$$E[g(N)] = \frac{M}{k-N+1} + \frac{M}{k-N+2} + ... + \frac{M}{k}.$$

From this equation, we can derive the following bounds.

$$\frac{M}{k} N \le E[g(N)] \le \frac{M}{k} \frac{N}{(1-\frac{N-1}{k})}.$$

The lower bound is obtained by replacing all terms in the above equation by $\frac{M}{k}$. The upper bound is obtained by replacing all terms in the above equation by $\frac{M}{k-N+1}$.

When the value of $N$ is very close to the value of $k$, the following relation holds:

$$\frac{M}{k-N+1} + \frac{M}{k-N+2} + ... + \frac{M}{k} \approx \frac{M}{k} N \log N.$$

Note that, as discussed before, $\frac{M}{k}$ is the expected test length for detecting the fault $f$ once.

The bounds derived in the previous paragraph can be explained intuitively. Since the patterns applied to the input of the circuit are random, some patterns may appear more than once before all possible patterns appear at the inputs. Suppose a fault is detected by a pattern which has appeared already; the number of times this fault is detected does not increase but stays the same. Hence, the expected test length for detecting a fault $N$ times by *different* test vectors is more than $N$ times the test length for detecting the fault only once.

Let us look at an actual circuit to understand the significance of the above bounds. Consider a combinational circuit with 14 inputs. Hence, $M$ = 16,384. Let us suppose that there is a fault $f$ in the circuit such that $f$ is detected by 96 input combinations. Therefore, $k$ = 96. This is not an unrealistic example because, the ALU 181 circuit has 14 inputs and there is a fault which is detected by only 96 input combinations [McCluskey 88]. The expected number of random patterns that we must apply to detect the fault $f$ once is equal to 171. Next, let us suppose that we want to detect this fault $f$ 5 times (i.e., $N$ = 5) – the expected random pattern test length lies between 855 and 892. If we want to detect the fault $f$ 20 times (i.e., $N$ = 20), the expected test length lies between 3420 and 4264. However, if the value of $k$ is 30 and $N$ is 20, the expected test length lies between 20 to 30 times the expected test length for detecting the fault only once.

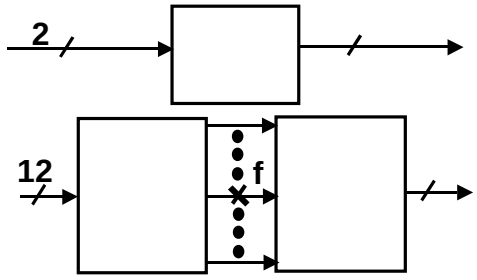


Figure 2. Illustration of Effective Detectability

Next, consider the following scenario. Suppose that, out of the 14 inputs of the given combinational logic circuit, values on only 12 inputs structurally affect the excitation and propagation of fault *f*. This means that, if we trace from the fault site of *f* to the primary outputs in the given logic network and then trace back from the primary outputs to the primary inputs, then we find that the primary outputs that can be affected by fault *f* depend on only 12 primary inputs. This is shown in Fig. 2. This means that, the values on the remaining 2 inputs do not affect the detection of the fault *f* structurally. If we have a gate-to-source short created by a gate-oxide short or an open defect at the fault site of *f*, we must be cautious and try to detect the fault *f* by applying different input combinations on the 12 inputs that really structurally affect the excitation and propagation of fault *f*. Continuing from our earlier example, suppose that the detectability of *f* is 96. In this scenario, we really have 24 (rather than 96) different choices of input combinations to detect the fault *f*. Thus, the *effective detectability* of the fault *f* for defects like gate-to-source shorts or opens at the fault site is 24.

Note that, defects like opens or gate-oxide shorts do not create extra dependence of any node in the circuit under test (CUT). Hence, the set of inputs of the CUT that affect the excitation and propagation of single stuck-at faults and contribute to the effective detectability of single-stuck-at faults for these detecting these kinds of defects can be found easily by traversing the given network. In contrast, for defects like interconnect shorts (shorts among different nodes in the given logic network), the problem of calculating the effective detectability of single stuck-at faults is more tricky. This is because, defects like interconnect shorts can create extra dependence on inputs which cannot be predicted without the knowledge about the actual defect. This problem can be addressed by using inductive fault analysis tools to generate a list of bridging defects that are highly probable.

By now, it must be clear that the value of effective detectability of a single stuck-at fault *f* depends on the defect type under consideration. This is clearly a new approach and introduces a "defect" component in the fault

grading of BIST patterns. Let $I$ be the set of all binary combinations that can be applied to the inputs that structurally affect the excitation and propagation of fault $f$ in a circuit $C$. The *effective detectability*, $d$, of the fault $f$ is defined as the number of members of $I$ that can detect $f$. If a combinational logic circuit has $m$ inputs and the excitation and propagation of a fault $f$ structurally depends on the values of only $t$ inputs, then $k = 2^{m-t}d$. In that case, our earlier equations are changed in the following way:

$$E[g(N)] = E[g(N-1)] + p_N + 2(1-p_N)p_N + 3(1-p_N)^2 p_N + \ldots.$$

where $p_N = \frac{k - [N-1]2^{m-t}}{M}$. This is because, when the fault $f$ will be detected $N$th time, none of the vectors with values same as the previous $N$-1 values on the $t$ inputs can be used. Hence, we have to get rid of $(N\text{-}1)2^{m-t}$ vectors out of the $k$ vectors that detect the fault $f$.

The above recurrence relation can be solved as follows:

$$E[g(N)] = E[g(N-1)] + \frac{1}{p_N}.$$

From this equation, we can derive the following bound.

$$\frac{M}{k}N \le E[g(N)] \le \frac{M}{k}\frac{N}{(1-\frac{[N-1]2^{m-t}}{k})}.$$

Hence,

$$\frac{M}{k}N \le E[g(N)] \le \frac{M}{k}\frac{N}{(1-\frac{[N-1]}{d})}$$

Note that, as discussed before, $\frac{M}{k}$ is still the expected test length for detecting the fault $f$ once.

If we want to detect $f$ with effective detectability equal to 24 ($d$ = 24 and $k$ = 96) 5 times, the expected test length can be as long as 1026. If we want to detect the fault 20 times, we could end up with a scenario where the expected test length can be approximately 40 times the test length for single detection.

As another example, let us suppose that the effective detectability of the fault $f$ is 6 (if $m$ = 14, $t$ = 10 and $k$ = 96); for detecting $f$ 5 times, the test length could be as high as approximately 9 times the test length for a single detection.

The following observations can be made from the above results:

1. For faults with very high values of effective detectability (after considering the structural dependence on inputs), the expected test length test length for $N$ detection is approximately $N$ times the expected test length for single detection. For example, if the effective detectability is 96 and $N$ is 5, then the expected test length is approximately 5 times the test length for single detection.
2. For the faults with very low values of effective detectability $d$ (after considering the structural dependence on inputs), the expected test length test length for $N$ detection is approximately $N\log N$ times the expected test length for single detection. For example, if the value of effective detectability is 24 and $N$ is 20, then the expected test length is approximately 40 times the test length for single detection. When $N$ is almost of the same order as of $d$, we can possibly use some techniques like mapping-logic [Touba 96] or test point insertion to actually apply the $N$ input combinations since we do not have a lot of choices for $N$ different input combinations; thus, we can reduce the test length for $N$ detection.
3. When the value of effective detectability is neither very high, nor very low, we have many possible choices of $N$ different input combinations (actually, there are $\binom{d}{N}$ such combinations). It is unknown and possibly hard to determine which set of $N$ different patterns to choose (unless we grade the different choices according to their surrogate fault-coverage [Butler 91]). In this scenario, we can possibly use a combination of weighted-random patterns [Waicukauski 89], mapping logic [Touba 96], test points and re-seeding of LFSRs to reduce the test length. We have not yet studied which combination of BIST techniques is most effective and it is outside the scope of this paper.

Although the results presented in this section are derived from theoretical calculations, we present simulation results in Sec. 4 to show that the above characteristics are true for real circuits in a pseudo-random BIST environment.

Our above analysis shows the relationship between the test lengths for single detection and $N$-detection of a single fault. However, in an actual BIST environment many single stuck-at faults have to be detected. Hence, the question is: what happens to the overall test length? Just like the case of single detection [McCluskey 88], for $N$-detection, the overall test length is dominated by the expected test length for the hard-to-detect faults with very low values of detectability and effective detectability.

## 4. Simulation Results

In this section, we present simulation results for a couple CUTs on the Murphy chip and the ELF35 chip [Ma 95][Li 99]. The Murphy chip is a 0.7um CMOS chip designed to evaluate the effectiveness of various test techniques. The ELF35 is a follow-up chip to the Murphy

chip. It was manufactured in 0.35um technology and is currently being tested.

Figure 3 shows the simulation flow. We first created the SSF dictionaries for all CUTs. Exhaustive patterns were applied to the CUTs to determine their detectability profiles. BIST test sets were generated by LFSRs with various initial seeds. Each BIST test set was then analyzed to count the number of times that each SSF was detected.

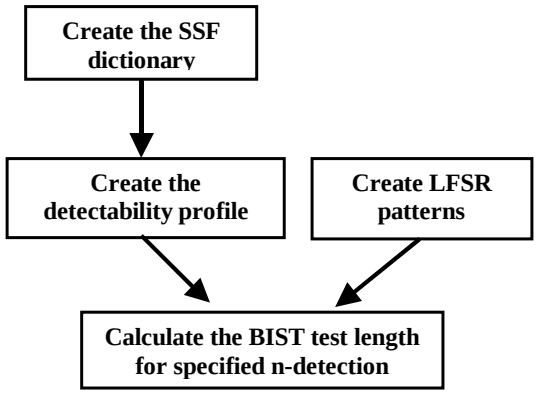


Figure 3. Simulation Flow

### 4.1 Pseudo-Random to Binary Translator

This CUT translates a pseudo-random sequence into a binary sequence. There are 398190 SSFs in this CUT. There are many faults with low detectability. Table 2 shows the detectability profile for faults with detectability less than 10.

Table 2: The detectability profile (detectability < 10)

| *k* | number of faults |
|---|---|
| 1 | 2179 |
| 2 | 3830 |
| 3 | 2799 |
| 4 | 1995 |
| 5 | 1564 |
| 7 | 1302 |
| 10 | 707 |

Table 3 shows a set of pseudo-random test fault simulation results using different seeds for the LFSR. Each entry represents the average ratio of test length for *N*-detection over 1-detection over all faults of a given detectability value. The results in Table 3 show that the test length increases more rapidly than linear as *N* approaches *k*, the detectability fault. As discussed earlier, we expect the test length to increase at a rate greater than *N* as *N* approaches k. Table 3 validates the predicted bound. For each entry, we show the bound calculated using our theoretical derivation in Sec. 3 within parenthesis. The upper bound was calculated using the actual expression for the expected test length for *N*-detection derived in Sec. 3. It can be seen that our theoretical predictions match the simulation results.

Table 3: Expected ratio of test length for the PB circuit

| *Detectability* | | *3* | *5* | *10* | *50* |
|---|---|---|---|---|---|
| *Number of faults* | | *2799* | *1564* | *707* | *70* |
| N = 1 | Seed 1 | 1 | 1 | 1 | 1 |
| | Seed 2 | 1 | 1 | 1 | 1 |
| | Seed 3 | 1 | 1 | 1 | 1 |
| N = 3 | Seed 1 | 3.6 (3, 5) | 3.1 (3, 4) | 3.3 (3, 3.4) | 3.1 (3, 3.1) |
| | Seed 2 | 3.4 (3, 5) | 3.2 (3, 4) | 3.5 (3, 3.4) | 3.3 (3, 3.1) |
| | Seed 3 | 3.3 (3, 5) | 3.5 (3, 4) | 2.9 (3, 3.4) | 3.4 (3, 3.1) |
| N = 5 | Seed 1 | NA | 6.9 (5, 11) | 5.6 (5, 6.4) | 4.9 (5, 5.2) |
| | Seed 2 | NA | 7.1 (5, 11) | 5.3 (5, 6.4) | 5.1 (5, 5.2) |
| | Seed 3 | NA | 7.2 (5, 11) | 5.4 (5, 6.4) | 5.5 (5, 5.2) |

### 4.2 Controller

This control circuit is part of a DMA controller. There are 7502 equivalent stuck-at faults in this CUT. The results in Table 4 also show that the test length increases linearly with the number of detections. This is because the number of detections, 1,3, and 5, are all small comparing with the detectability, 12, 20, 50, and 100. For each entry, we show the bound calculated using our theoretical derivation in Sec. 3 within parenthesis. The results match our theoretical predictions.

Table 4: Average test length for the controller circuit

| ***Detectability*** | | ***12*** | ***20*** | ***50*** | ***100*** |
|---|---|---|---|---|---|
| *Number of faults* | | *23* | *120* | *76* | *144* |
| N=1 | Seed 1 | 1 | 1 | 1 | 1 |
| | Seed 2 | 1 | 1 | 1 | 1 |
| | Seed 3 | 1 | 1 | 1 | 1 |
| N=3 | Seed 1 | 2.87 (3, 3.3) | 2.75 (3, 3.2) | 2.97 (3, 3.1) | 3.43 (3, 3) |
| | Seed 2 | 2.75 (3, 3.3) | 2.64 (3, 3.2) | 3.23 (3, 3.1) | 3.23 (3, 3) |
| | Seed 3 | 3.34 (3, 3.3) | 2.93 (3, 3.2) | 3.14 (3, 3.1) | 3.09 (3, 3) |
| N=5 | Seed 1 | 5.43 (5, 6) | 5.22 (5, 5.6) | 4.73 (5, 5.2) | 5.51 (5, 5.1) |
| | Seed 2 | 5.19 (5, 6) | 5.25 (5, 5.6) | 5.14 (5, 5.2) | 5.73 (5, 5.1) |
| | Seed 3 | 5.55 (5, 6) | 5.02 (5, 5.6) | 5.21 (5, 5.2) | 5.49 (5, 5.1) |

## 5. Conclusions and Future Directions

In this paper, we analyzed the effectiveness of pseudo random testing for detecting real defects by using the concept of single stuck-at fault *N*-detect coverage as a metric to determine the quality of the pseudo-random test patterns. We introduced the idea of effective detectability and theoretically derived bounds on the minimum test

length of random or pseudo-random patterns required to achieve a given *N*-detect coverage. For faults with high values of effective detectability, the expected test length for *N*-detection is around *N* times the expected test length for single detection. However, for faults with low effective detectability, the expected test length for *N*-detection can be *N*log*N* times the expected test length for detecting the fault only once; this increases the test length significantly.

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### Appendix A: Expected *N*-detect Test Length for Pseudo-Random Patterns

In this section, we derive the expressions for the probability that a fault is detected ***N*** times by a pseudo-random test sequence of length ***L***. We assume that the pseudo-random test sequence is generated by an ***m-bit*** LFSR. We also assume that the LSFR can generate all the possible $M = 2^m$ patterns, i.e., the LFSR has been modified to include the all-0 pattern.

**Theorem 1**: The probability that a fault of detectability with ***k*** is detected exactly *x* times ($x \le L$, $x \le k$) in a pseudo-random test sequence of length ***L*** is

$$Q(x,M,L,k) = \frac{C_x^k \times C_{L-x}^{M-k}}{C_L^M} = \binom{L}{x} \frac{[\prod_{i=0}^{x-1}(k-i)][\prod_{i=0}^{L-x-1}(M-k-i)]}{\prod_{i=0}^{L-1}(M-i)}$$

***Proof***: In pseudo random testing, each test vector is chosen with equal probability out of a "pool" that initially contains ***M*** different vectors and "not" replaced [Wagner 86]. The first term in the nominator is the number of ways to choose *x* out k detecting patterns. The second term in the numerator is the number of ways to choose (*L-x*) out of the remaining (*M-k*) non-detecting patterns. Their product represents the number of test sequences of length *L* that contain *x* detecting patterns and (*L-x*) non-detecting patterns. The denominator of is the number of ways to choose *L* patterns from all of the *M* possible LFSR patterns. Therefore, their ratio is the probability that the fault is detected exactly x times in the pseudo-random test sequence. **Q.E.D.**

Theorem 1 shows that the number of times that a fault is detected in a pseudo-random sequence is a hyper-geometric random variable. The next theorem derives the expression of the expected length of a pseudo-random sequence for detecting a fault *N* times.

**Theorem 2:** For a fault of detectability *k (k>=N)* the probability that a fault is not detected N times until the L-th vector in a pseudo-random sequence, i.e., the L-th pattern is one of the ***N*** detecting patterns, is

***Proof***: The first term is directly adopted from Theorem 1 with ***x=N***. It represents the probability that the fault is detected *N* times in a pseudo-random sequence of length *L*.

$$\frac{C_N^k \times C_{L-N}^{M-k}}{C_L^M} \times \frac{N}{L}$$

It is the sum of the probabilities of two excluding events: 1. the *L-th* pattern is a detecting pattern and 2. the *L-th* pattern is not a detecting pattern. It is the probability of event 1 that we are trying to derive. The percentage of event 1 is the conditional probability that the L-th pattern is a detecting pattern when there are N detecting patterns in the L patterns. The conditional probability is N/L.

**Q.E.D.**

Combining Thm 1 and 2, the expected length *E(L)* of a pseudo-random sequence for detecting the fault N times is

$$E(L) = \sum_L \Pr(Length = L) \times L =$$

$$\sum_{L=N}^{M} \frac{C_N^k \times C_{L-N}^{M-k}}{C_L^M} \times \frac{N}{L} \times L = N \times C_N^k \times \sum_{L=N}^{M-k+N} \frac{C_{L-N}^{M-k}}{C_L^M}$$