Error Sequence Analysis on Transition Fault Patterns

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Outline
- Introduction
- Advantages
- Test Result
- Summary

Basic Idea
- Error Sequence
  - Sequence of erroneous output according to its failing frequency.
- Error Sequence Analysis
  - Analyzing error sequence to find small delay flaws

Error Sequence
- Frequency Sweep (100MHz to 120MHz)
- Frequency: 100MHz

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Output @ 100MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>P1 P2 P3 P4</td>
</tr>
<tr>
<td>01</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>02</td>
<td>1 1 1 0</td>
</tr>
<tr>
<td>Circuit</td>
<td>0 1 0 1 0</td>
</tr>
<tr>
<td>04</td>
<td>1 1 0 1</td>
</tr>
<tr>
<td>05</td>
<td>0 0 1 0</td>
</tr>
</tbody>
</table>

Error Sequence
- Frequency Sweep (100MHz to 120MHz)
- Frequency: 110MHz

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Output @ 110MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>P1 P2 P3 P4</td>
</tr>
<tr>
<td>01</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>02</td>
<td>1 1 1 0</td>
</tr>
<tr>
<td>Circuit</td>
<td>0 1 0 1 0</td>
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<tr>
<td>04</td>
<td>1 1 0 1</td>
</tr>
<tr>
<td>05</td>
<td>0 0 1 0</td>
</tr>
</tbody>
</table>

Error Sequence
- Frequency Sweep (100MHz to 120MHz)
- Frequency: 120MHz

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Output @ 120MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>P1 P2 P3 P4</td>
</tr>
<tr>
<td>01</td>
<td>0 1 0 0</td>
</tr>
<tr>
<td>02</td>
<td>1 1 1 0</td>
</tr>
<tr>
<td>Circuit</td>
<td>0 1 0 1 0</td>
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<td>04</td>
<td>1 1 0 1</td>
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<tr>
<td>05</td>
<td>0 0 1 0</td>
</tr>
</tbody>
</table>

Error B (P1, O3) @120MHz
Error C (P3, O4) @120MHz
Error A (P2, O2) @110MHz
Introduction

- Error Sequence Analysis
  - Method
    - Error sequence generation by frequency sweep
    - Error sequence comparison with good chip
  - Objective
    - Detecting small delay flaws
      (delay size < propagation path slack)
  - Purpose
    - NTF analysis / Characterization test

Example: no defect

Example: with delay defect

Advantages

- Pattern generation time
  - Using transition-fault model
  - Smaller than path-delay fault model
- Robust to global process variation
  - lot-to-lot, wafer-to-wafer

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Example

- Small delay fault
  - at block A (0.2ns)
- Transition fault
  - Propagation path
  - A:B
  - With fault
    - A:B : 0.9ns < 1.0ns (Not detected)
    - A:C : 1.1ns > 1.0ns (Undetected error)
Example

Error Sequence Analysis
- Propagation path:
  - A:B (0.7ns < 0.9ns)
  - D:E (0.8ns)
- Without fault:
  - A:B < D:E
- With fault:
  - A:B > D:E
- Different sequence

Process Variation

Minimum Operating VSD vs. Device Speed

Without fault:
A:B < D:E
Different sequence

With fault:
A:B > D:E
Different sequence

Error Sequence Analysis

Process Variation
- Within die << Die-to-Die << Wafer-to-Wafer
- Retaining sequence

Error Sequence Analysis

In spite of process variation
- Changing sequence due to small delay
  - Error free: a → b → c
  - Erroneous: a → c → b

Outline

Introduction
Advantages
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Previous ELF18 Test

Number of Samples
- 88 cores
Objective
- Checking regularity of error sequence
Pattern
- 13 Super patterns
Results
- 3 suspects out of 88 cores
ELF18 Test

- Number of Samples
  - 472 cores
- Transition fault pattern
  - Length: 1417, Fault coverage: 97%
- Step size
  - 0.1ns (100ps)
- Range
  - 10 sweeps from first failing period

Good chip results (Pin = DIG_Q1)
- All good cores

<table>
<thead>
<tr>
<th>Pin</th>
<th>059</th>
<th>060</th>
<th>061</th>
<th>062</th>
<th>063</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pat. 73</td>
<td>86%</td>
<td>72%</td>
<td>96%</td>
<td>90%</td>
<td>95%</td>
</tr>
<tr>
<td>Pat. 616</td>
<td>4%</td>
<td>96%</td>
<td>84%</td>
<td>22%</td>
<td></td>
</tr>
<tr>
<td>Pat. 1058</td>
<td>80%</td>
<td>38%</td>
<td>96%</td>
<td>45%</td>
<td></td>
</tr>
<tr>
<td>Pat. 1172</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td></td>
</tr>
<tr>
<td>Pat. 1214</td>
<td>20%</td>
<td>72%</td>
<td>68%</td>
<td>81%</td>
<td></td>
</tr>
</tbody>
</table>

Ex) Pat. 73 fails earlier than Pat. 616 with frequency of 86.4%

Bad chip results (Pin = DIG_Q1)
- Good cores: 152, Bad cores: 70
- Lesser regularity than good chip result

Finding first failing period
- Binary search method

Good chip results (other pins)

<table>
<thead>
<tr>
<th>Pin</th>
<th>059</th>
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<th>062</th>
<th>063</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pat. 73</td>
<td>54%</td>
<td>90%</td>
<td>96%</td>
<td>40%</td>
<td>60%</td>
</tr>
<tr>
<td>Pat. 616</td>
<td>56%</td>
<td>96%</td>
<td>90%</td>
<td>40%</td>
<td>60%</td>
</tr>
<tr>
<td>Pat. 1058</td>
<td>33%</td>
<td>96%</td>
<td>57%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pat. 1172</td>
<td>0%</td>
<td>0%</td>
<td>0%</td>
<td>13%</td>
<td></td>
</tr>
<tr>
<td>Pat. 1214</td>
<td>31%</td>
<td>47%</td>
<td>31%</td>
<td>81%</td>
<td></td>
</tr>
</tbody>
</table>

Bad chip results (other pins)
ELF18 Test

- Overall results (Pin = DIG_Q1)
  - Good cores: 402, Bad cores: 70

<table>
<thead>
<tr>
<th>Pin</th>
<th>84.5%</th>
<th>74.4%</th>
<th>95.6%</th>
<th>90.47%</th>
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<tbody>
<tr>
<td>73</td>
<td></td>
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</tr>
<tr>
<td>616</td>
<td>45.7%</td>
<td>38.4%</td>
<td>83.2%</td>
<td>31.4%</td>
</tr>
<tr>
<td>1058</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1172</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>1214</td>
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<td></td>
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</tbody>
</table>

ELF18 Test

- Overall results (other pins)

<table>
<thead>
<tr>
<th>Pin</th>
<th>84.7%</th>
<th>36.4%</th>
<th>95.6%</th>
<th>53.7%</th>
</tr>
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<tbody>
<tr>
<td>1058</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1172</td>
<td>45.6%</td>
<td>64.2%</td>
<td>0%</td>
<td>10%</td>
</tr>
<tr>
<td>1214</td>
<td>25.4%</td>
<td>60.9%</td>
<td>48.7%</td>
<td>81.4%</td>
</tr>
</tbody>
</table>

ELF18 Test

- Suspects
  - 13 cores out of 472 cores
  - Fewer than transition pattern test fails
  - Why?

ELF18 Test

- First failing period of cores
  - Core 20 ~ core 30 (395 cores)

ELF18 Test

- Using error sequence analysis
  - Detecting real delay defects
Outline

- Introduction
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Summary

- Error Sequence Analysis
  - Small delay detection by error sequence comparison
- Advantages
  - Robust to global die variation
  - Using transition fault model
- ELF18 Test
  - Useful to detect real delay defective cores
- Purpose
  - NTF analysis / characterization test