Failing Frequency Signature

Jaekwang (Jake) Lee
Center for Reliable Computing (CRC)
Department of Electrical Engineering
Stanford University

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Outline

- Introduction
- Failing Frequency Signature vs. Error Sequence
- Test Result
- Conclusion

Definitions

- Frequency Sweep
  - Test application at various clock frequencies (low to high)
- Failing Frequency
  - Minimum frequency with erroneous output
- Failing Frequency Signature
  - Collection of failing frequency of each pattern in the pattern set

Example

- Failing Frequency Signature (3 patterns)
- With delay defect

Example

- Failing Frequency Signature (3 patterns)
- Good device (reference)

Failing Frequency Signature

- Obtaining Failing Frequency Signature
  - Failing frequency of each pattern using frequency sweep
- Analyzing Failing Frequency Signature
  - Frequency version of IDDQ signature
  - Exploiting IDDQ researches
    - Current Signature [Gattiker 96]
    - Delta-IDDQ [Thibeault 97]
    - Current ratios [Maxwell 99]
Failing Frequency Signature

- Objectives
  - Detecting small delay defects
  - Better than Error Sequence Analysis
  - Better resolution
  - Reduced test time
  - Reduced storage requirement

- Purpose
  - NTF analysis
  - Characterization test

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Review: Error Sequence Analysis

- Error Sequence
  - Frequency sweep test with a pattern set
  - Sequence of erroneous output according to its failing frequency

- Error Sequence Analysis
  - Error sequence comparison with good chip's sequence

Review: Error Sequence

- Frequency Sweep (100MHz to 120MHz)
  - Test frequency: 100MHz
  - Error A (P2, O2) at 110MHz
  - Error B (P1, O3) at 120MHz
  - Error C (P3, O4) at 120MHz

- Error Sequence
  - Frequency Sweep (100MHz to 120MHz)
  - Test frequency: 120MHz
  - Error A (P2, O2) at 110MHz
**Review : Example**

- **Small delay fault**
  - At block A (0.2ns)

- **Transition fault**
  - Propagation path
  - A? B
  - With fault
    - A? B : 0.8ns < 1.0ns (Not detected)
    - A? C : 1.1ns > 1.0ns (Undetected error)

**Error Sequence Analysis**

- Propagation path
  - A? B (0.8ns ? 0.8ns)
  - D? E (0.7ns)

- Without fault
  - A? B < D? E

- With fault
  - A? B > D? E
  - Different sequence

**Failing Frequency Signature vs. Error Sequence**

- **Same**
  - Using frequency sweep
  - Robust to lot-to-lot, wafer-to-wafer process variation

- **Different**
  - Pattern application
    - Single pattern vs. pattern set
  - Issues
    - Test time
    - Resolution
    - Storage requirement

**Robust to Global Process Variation**

- **Process variation**
  - Within die << Die-to-Die << Wafer-to-Wafer
  - Retaining signature

**Issue : Test time**

- **Finding Failing Frequency (or Period)**
  - Binary search method

- **Example**
  - Range : 12ns, Resolution < 0.1ns
  - Number of different freq. application = 7

- Test time compared to transition test
  - Expectation : around 20 times
  - Real application : Much greater!! (50~60 times)
**Issue : Test Time & Resolution**

- ELF18 transition fault test pattern
  - Longest sensitized path : 9.27ns
  - Shortest sensitized path : 2.70ns
- Desired resolution : < 0.5ns
  - Error sequence analysis
    - \((9.27 - 2.70) / 0.5 = 13.14 \rightarrow 14\)
  - Failing frequency signature
    - \(\log_2(9.27 - 2.70) / 0.5 = 3.72 \rightarrow 4\)

**Issue : Storage Requirement**

- Less than error sequence analysis
  - 3 pattern set example

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**ELF18 Test**

- Number of Samples
  - 36 cores
- Transition test set
  - Number of patterns : 1417
  - Fault coverage : 97%
- Clock period
  - Range : 2ns ~ 14ns
  - Resolution : 0.1ns

**Frequency Signatures**

- Good Chip
- Bad Chip
**Frequency Signatures**

- **Suspect**

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**Conclusion**

- **Failing Frequency Signature Analysis**
  - Small delay flaw detection
- **Advantages over Error Sequence Analysis**
  - Better resolution
  - Less storage requirement
  - Exploiting IDDQ analysis method
- **Issue**
  - Test time: much longer than expected time
- **Purpose**
  - NTF analysis / characterization test

**References**