Digital IC Testing for Art Historians and Test Experts

E.J. McCluskey
October 11, 2004

Acknowledgements

- Mike Purtell, Sassan Raissi, Phil Nigh
- THE RATS

Outline

- Production Testing
- Basic Concerns
- Defect Effects (Modes) and Failure Causes
- Common Wisdom - Myths
  - Evidence - the ELF Experiments
- Issues
  - More Myths
- The Future

Conclusions

- Affordable, adequate production testing
  - Novel access circuitry
  - Better, proven test metrics
  - Lucky accident ?
  - OR
  - FUNDAMENTAL RESEARCH RESULT ?
- Research funding can make it happen!
Production Testing

- Every chip or a sample of the chips tested
  - Defective chips discarded

- Test quality
  - How many defective chips are passed

AH question
What if test procedure is faulty?

Production Test

- Input signals applied
  - Correctness of response verified, or
  - Speed of correct operation determined

- Test Conditions controlled
  - Temperature
  - Speed
  - Voltage value

Other Test Procedures

- Quality assurance test
  - Very thorough test of chip sample

- Diagnostic test
  - Test to determine failure cause

- Reliability test
  - Test to estimate useful lifetime

- Weak parts test
  - Test to identify chips with very short lifetimes

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    - Quality, Test Cost, Access

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The Basic Concerns

- Quality
  - Too low,
  - Hard to measure

- Testing cost
  - Too high,
  - Increasing fraction of chip manufacturing cost

Cost of Test

Gelsinger, IEEE Design & Test, Jan. 2000, CTO, Intel
The Basic Concerns - Causes

- Low quality – test not thorough enough
  - Inadequate access
- Too expensive – test too long
  - Inadequate access

Access

1960s
- 7400 SSI IC
  - 12 logic pins (I/Os), 4 gates
  - 0.33 gate/pin ratio

2000s
- nVIDIA Graphics Processor
  - ≈ 400 logic pins (I/Os), 4 million gates
  - ≈ 10 thousand gates/pin ratio

7400 SSI IC

logic diagram

package

nVIDIA Graphics Processor

Inadequate Access

- Gate to Pin ratio
  - Steady growth
- Solutions?
  - Increase access
    - Test points – observability, controllability
    - Scan – full vs. partial
    - “Scanout”
    - SOC partitions and wrappers
    - BIST

Can’t keep up!

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Defect Effects (Modes)

- Defective chip aberrant behavior
  - Incorrect output signal values
  - Input signal changes slow to reach output
  - Invalid output signal values
- Observable on tester or test fixture

THAT'S ALL!

Failure Causes

- Failure causes
  - Defective chip structural anomaly
    - Extra or missing connections
    - Connection resistance incorrect

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Common Wisdom - Myth number 1

- Myth number 1
  - Each new technology has
    - New, mysterious failure modes
    - Need new, more complex fault models

New failure modes will require new failure models, Wally Rhines, Mentor Graphics CEO, Keynote speech 2003

Common Wisdom - Myth number 1

- The truth
  - Failure effects (modes) aren't changing
  - Failure causes may change
  - Population of defect types may change
  - Sensitivity to test conditions may change
- Needed
  - Better metrics, more effective test conditions
- Fault models
  - Very important for DIAGNOSIS
  - Not the issue for production test
- Test Metrics
  - Very important for PRODUCTION TEST

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### Evidence – the ELF Experiments

- Murphy 1991 Hughes Aircraft Custom Chip
- ELF 35 1996 LSI Logic Custom Chip
- ELF 18 2002 Philips Test Chip
- NV 18 2004 nVidia Graphics Processor

### Murphy Chip

- LSI Logic 150K CMOS Gate Array
- 25K Gate design
- $L_{eff} = 0.7 \, \mu m$
- Nominal VDD = 5v
- 5 Combinational Cores
  - 4 Copies of each core
- Support DFT circuitry

### ELF35 Chip

- LSI Logic G10P technology
- $L_{eff} = 0.35 \, \mu m$
- Nominal VDD = 3.3v
- 6 Cores
  - 4 Combinational Cores
    - 1 translator, 3 datapath
  - 2 Sequential (2901’s)
    - full scan

### MURPHY Time Line

- 1991: Project started
- 1993: Design completed
- 1995: Wafer sort results, ITC
- 1997: Package chips received
- 1998: Package test results, VTS
- 2000: Burn-in results, ITC

### ELF35 Time Line

- Jan. 1996: Project started
- Nov. 1996: Logic Design Completed
- Apr. 1997: Tape-out
- Jun. 1997: First silicon
- 1998: Test Patterns Collected
- 1999: Test Program Debug
- Nov. 2000: 3,000+ chips received
- Aug. 2001: 6,000+ chips received
- Mar. 2002: All chips tested
- Jun. 2003: Interesting chips studied

### ELF18

- 0.18 \, \mu m technology
- 12 Million transistors
- 6 interconnect layers
- Area 30 mm²
- 80 IO pins
- 6 DSP cores
nVIDIA Graphics Processor

- 0.14 μm technology
- 34 Million transistors
- 7 interconnect layers
- Area 8.49mm*8.49mm
- 403 IO signal pins

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Defect Classification

Combinational defect
  - Response to pattern n
    - Independent of pattern n-1
Timming dependent defect
  - Response to patterns
    - Dependent on pattern speed
Sequence dependent defect
  - Response to patterns
    - Dependent on pattern order

Defect Classification

Single stuck-at faults
  - Tester output = SSF fault simulation output?
  - Perfect match
    - Defect = SS@
  - Test set used
    - 100% SSF test set

Defect Classification

TIC defect
  - Timing independent combinational defect
    - Reorder patterns ⇒ no change in results
    - Change test speed ⇒ no change in results
**Sequence Dependent Defects**
- Sequence dependent defect
  - Single stuck defect: NO
  - Multiple stuck defect: NO
  - Non-feedback bridging defect: NO
  - Stuck open: possibly
  - Feedback bridging: possibly
  - Delay defect: possibly

**Timing Dependent Defects**
- Same test set
  - Defect detected at one speed
  - Escapes at another speed
- Possible causes
  - Resistive opens
  - Process variation

**Defect Classification**

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**Issues**
- 1. Testing vs. Diagnosis
- 2. Which input patterns?
- 3. Metrics vs. Models

**Issue 1: Testing vs. Diagnosis**
- Testing
  - Identify broken CHIPS
- Diagnosis
  - Identify DEFECT in broken chip
    - Done on only a sample

Focus here is on Testing
### Testing Techniques

- **Functional test**
  - Mimic chip operation in product
  - Fixture
    - ATE (chip tester) or
    - Product sockets

- **Structural test**
  - ATE (chip tester)
    - Verify chip structure

### Issue 2: which input patterns?

- **Functional test**
  - Patterns from chip operation in product
    - Same as in chip application
    - Too many patterns
    - Not a thorough test

  - Design verification patterns
    - Not a thorough test
    - Patterns must be augmented
    - Not automated, very expensive

### Issue 2: which input patterns

- **Structural test**
  - Verify chip structure
  - Too many possible input patterns
    - How to choose?
    - Metric needed

### Issue 3 - Models vs. Metrics

- **Model**
  - Representation at logic, circuit or physical level
    - Effect of defect on chip behavior
  - Vital for diagnosis

- **Metric**
  - Measure of test completeness
  - Used
    - To guide test set generation
    - To assess test set completeness

Metric most important for testing

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### Fault Models

- Single stuck-at fault
- Bridging fault – wired logic
- Bridging fault – dominant net
- Delay fault
- Stuck-open fault

### Test Metric

- Specify procedure to:
  1. Guide selection of input patterns (test set) to:
    - activate aberrant behavior, and
    - sensitize incorrect signal to output (optional)
  2. Estimate completeness of test set
    - in achieving these goals
  3. Specify test conditions (optional)
Test metrics

- Toggle test – static, dynamic (Single or Double)
- Single stuck fault
- Transition test
- Taro
- N-Detect test
- Gate exhaustive
- Pseudo stuck fault

Static Toggle Test Metric

- Guide test set selection
  - Try to place both 0 and 1 on each node
- Grade generated test set
  - Fraction of nodes that receive both 0 and 1

Toggle Test Metric Example

<table>
<thead>
<tr>
<th>Input</th>
<th>Output</th>
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</thead>
<tbody>
<tr>
<td>A</td>
<td>0 1</td>
</tr>
<tr>
<td>S</td>
<td>0 1</td>
</tr>
<tr>
<td>B</td>
<td>0 1</td>
</tr>
<tr>
<td>A &amp; S</td>
<td>0 1</td>
</tr>
<tr>
<td>S &amp; B</td>
<td>0 1</td>
</tr>
<tr>
<td>&amp;</td>
<td>0 1</td>
</tr>
<tr>
<td>+</td>
<td>0 1</td>
</tr>
<tr>
<td>Z</td>
<td>0 1</td>
</tr>
</tbody>
</table>

- 83% Toggle Coverage

What we learned from Murphy-Elf

- Which output the incorrect signal reaches
  - Very important – Taro
- Two different input patterns
  - The same activation and sensitization
  - Different test effectiveness – N-detect

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Common Wisdom- Myth Number 2

- Exhaustive test of combinational circuit
  - All input patterns
  - Detects all defects
- The truth
  - Pattern sequence matters
  - Some defects insert state

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**Evidence - Murphy Tester Data**

- Exhaustive test failure data

<table>
<thead>
<tr>
<th>Coverage</th>
<th>Rated Speed</th>
<th>Slow Speed</th>
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</thead>
<tbody>
<tr>
<td>80%</td>
<td>7</td>
<td>2</td>
</tr>
<tr>
<td>90%</td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>95%</td>
<td>5</td>
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<td>2</td>
<td>1</td>
</tr>
<tr>
<td>Exhaustive</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

**Common Wisdom- Myth Number 3**

- Detection of “un-modeled faults” (defects)
  - Good measure of test quality
- The truth
  - Modeled faults means single stuck faults
  - Almost all defect behavior
    - Not like single-stuck fault
    - ELF35 5%, Murphy 35%

**Defect Classification**

**Common Wisdom- Myth number 4**

- Transition tests necessary
  - Only for timing defects
- The truth
  - Pattern sequence matters
  - Some defects insert state

**Common Wisdom- Myth Number 5**

- Thorough (high quality) Test
  - Patterns from several metrics
- The truth
  - Complete metric
    - May still be found

**Common Wisdom- Myth Number 6**

- Thorough (high quality) Test
  - Must target timing failures
- The truth
  - Absolutely correct
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The Future

- Access a growing problem
  - Gate to Pin ratios continue to rise
- Test set size continues to rise

The Future - Fixes

- Access
  - More internal access circuitry
  - Another SOC-like level
  - More test points
  - Concurrent Error Detection or Correction
  - BIST – Mixed mode

The Future - fixes

- Test set size
  - More efficient test sets
    - Better test metrics
  - Concurrent Error Detection or Correction

Number of Logic Transistors per Pin

<table>
<thead>
<tr>
<th></th>
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<th></th>
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<tbody>
<tr>
<td>Value</td>
<td>0</td>
<td>20,000</td>
<td>40,000</td>
<td>60,000</td>
<td>80,000</td>
<td>100,000</td>
<td>120,000</td>
<td>140,000</td>
</tr>
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</table>

Compiled from ITRS 1999 Data

Stimulus Test Pattern Size

<table>
<thead>
<tr>
<th>Year</th>
<th>2000</th>
<th>2005</th>
<th>2010</th>
<th>2015</th>
<th>2020</th>
</tr>
</thead>
<tbody>
<tr>
<td>GBit</td>
<td>0</td>
<td>20</td>
<td>40</td>
<td>60</td>
<td>80</td>
</tr>
</tbody>
</table>

Compiled from ITRS 2003 Data
Conclusions

- Affordable, adequate production testing
  - Novel access circuitry
  - Better, proven test metrics
  
  Lucky accident?
  OR
  FUNDAMENTAL RESEARCH RESULT?

- Research funding can make it happen!