Testing Digital Circuits with Constraints

Ahmad Al-Yamani, Stanford CRC
Subhasish Mitra, Intel
Edward J. McCluskey, Stanford CRC

Presented by: Nur Touba, UT Austin
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Purpose

- Pseudorandom Testing
  - Digital Circuits with Constraints on Signals
    - e.g. One-hot signals
Outline

- Background
- Previous work
- Illegal state detection
- Fixing illegal states
- Skipping illegal states
- Results
- Summary and Conclusion
One-Hot Signals

- **One-Hot Condition**
  - Exactly one signal active at a time

- **Multiple-Hot Problem**
  - Multiple lines driving output
    - CONTENTION

- **Zero-Hot Problem**
  - No line driving output
    - Floating output
One-Hot Signals Sources

- **Busses**
  - Controlled by tri-state drivers

- **N-to-1 Selectors**
  - Implemented with N transmission gates

- **Scan-based pseudorandom test**
  - One-hot condition may not be satisfied
Example

<table>
<thead>
<tr>
<th>E_1</th>
<th>E_2</th>
<th>I_1</th>
<th>I_2</th>
<th>O</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td>✓</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>✓</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>?</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>
Problem Definition

- Scan-based Pseudorandom Testing
  - Ensure one-hot signals
    - Scan and Capture cycles
    - No fault coverage loss
Scan Operation

- Standard fix for one-hot signals
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Previous Work

- Priority encoder [Fleming92, Mitra97]
  - Insert a priority encoder at the 1-hot signals
  - Delay 😞
    - Several levels of logic
  - Specific to 1-hot problem 😞
Previous Work

- Fixed value throughout test
  - [Levitt95, Hetherington99, Raina00]
    - Fault coverage 😞

```
Test Mode

Bus

E1  E2  E3  E4
```
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Illegal State Detection (ISD-Trace)

- ISD in terms of PIs and FFs
  - Back trace one-hots to PIs and FFs
    - $E_1 = F_1(\text{PIs, FFs})$
    - $E_2 = F_2(\text{PIs, FFs})$
    - $E_3 = F_3(\text{PIs, FFs})$
  - ISD = $(F_1F_2\bar{F}_3 + F_1\bar{F}_2F_3 + F_1\bar{F}_2\bar{F}_3)$
ISD-BIST

- BIST
- Test set known
- ISD-BIST
  - Logical Sum of patterns causing illegal values
    - Logic simulation

\[ ISD = \sum (\text{IllegalPatterns}) \]
ISD with BIST

Combinational Logic

Fixing Logic

Scan Chain

Pattern Counter

Bit Counter

Control Signals Generator

SE & TM

ISD

PRPG

MISR

PIs

POs

Control Signals Generator

Pattern Counter

Bit Counter

Fixing Logic

Combinational Logic

ISD with BIST

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Fixing Logic

ISD Circuit

Bistables

PIs

TM

SE

Bus

E1

E2

E3

E4

Fixing logic
ISD + Fixing Logic

- Small delay 😊
- During scan-in, scan-out and capture 😊
- No fault coverage sacrifice 😊
- Small ISD ⇒ low area overhead 😊

But …

- Delay 😞
- Design change 😞
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ISD with Extra FFs

- Use “bit counter” from BIST controller
Skip Illegal Patterns

- Instead of fixing logic
  - Skip bad patterns
- Change SE
- Use bit counter
Outline

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Benchmark

<table>
<thead>
<tr>
<th>PIs</th>
<th>POs</th>
<th>InOuts</th>
<th>Bistables</th>
<th>Busses</th>
<th>Area</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>88</td>
<td>176</td>
<td>508</td>
<td>6</td>
<td>29817</td>
</tr>
</tbody>
</table>

- Only benchmark with tri-state drivers
## Results

<table>
<thead>
<tr>
<th>Busses</th>
<th>Bus width</th>
<th>Tri-state drivers</th>
<th>ISD circuit area</th>
<th>%Area overhead</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus 1</td>
<td>17</td>
<td>2</td>
<td>10</td>
<td>0.034</td>
</tr>
<tr>
<td>Bus 2</td>
<td>17</td>
<td>2</td>
<td>10</td>
<td>0.034</td>
</tr>
<tr>
<td>Bus 3</td>
<td>6</td>
<td>3</td>
<td>40</td>
<td>0.134</td>
</tr>
<tr>
<td>Bus 4</td>
<td>6</td>
<td>5</td>
<td>82</td>
<td>0.275</td>
</tr>
<tr>
<td>Bus 5</td>
<td>6</td>
<td>7</td>
<td>93</td>
<td>0.312</td>
</tr>
<tr>
<td>Bus 6</td>
<td>6</td>
<td>3</td>
<td>31</td>
<td>0.104</td>
</tr>
</tbody>
</table>

*ISCAS benchmarks results in paper and TR*
Outline

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Summary

- ISD technique applicability
  - IC production, board-level and system-level
- No fault coverage sacrifice
- Non-intrusive
- Very low area overhead
- Very low delay overhead
- Applicable with BIST
- Any constraints, not only one-hot
Conclusion

- Pseudorandom Test
  - One-Hot constraints on signals
  - Efficient and practical solution
References