Testing Digital Circuits with Illegal States

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November 19, 2001

Motivation

- Digital Circuits with Constraints
  - One-hot
    - Pass-transistor Logic
    - Tri-state buffers
  - Scan-based Testing
  - Pseudo Random Testing
Objective

- Illegal State Detection (ISD) and Fixing
  - Minimal area overhead
  - Minimal delay overhead
  - No fault coverage sacrifice
  - General applicability
    - Production
    - Board level
    - System level

Problem Definition

- Normal operation ✓
- Scan-based or Pseudo-random test ?

<table>
<thead>
<tr>
<th></th>
<th>E1</th>
<th>E2</th>
<th>I1</th>
<th>I2</th>
<th>O</th>
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<tbody>
<tr>
<td>e</td>
<td>e`</td>
<td>x</td>
<td>x</td>
<td></td>
<td>✓</td>
</tr>
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<td>1</td>
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<td>a</td>
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<td>x</td>
<td>x</td>
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Previous Work

- One-hot latches
  - Remove from scan chain [1]
    - Sequential TPG
- Force static value during scan [3,4,6,7]
  - How about capture cycle?
  - Fault coverage
- Priority encoder [2,5]
  - Delay

Illegal State Detection (ISD)

- ISD in terms of PIs and FFs
  - Simulate all inputs
  - Back trace one-hots to PIs and FFs
    - Add the non-one-hot detection circuitry
    - $E_1 = F_1(\text{PIs, FFs})$
    - $E_2 = F_2(\text{PIs, FFs})$
    - $E_3 = F_3(\text{PIs, FFs})$
    - $\text{ISD} = (F_1F_2\bar{F_3} + F_1\bar{F_2}F_3 + F_1\bar{F_2}\bar{F_3})$
Fixing Logic

ISD + Fixing Logic

- Small delay
- During scan-in, scan-out and capture
- No fault coverage sacrifice
- Small ISD ⇒ low area overhead

But ...
- Delay
- Design change
ISD with BIST

P R P G

Control Signals Generator

Pattern Counter

Bit Counter

LBIST Controller

Combinational Logic

Fixing Logic

Scan Chain

MISR

ISD

PRPG

SE & TM

ISD

ISD with Extra FFs

Use “bit counter” from BIST controller

BIST Controller

Control Signals Generator

PRPG

Bit Counter

TM

SE

Fixing Logic

Control Logic

FFS

ISD

Circuit Under Test
Skip Illegal Patterns

- Instead of fixing logic
  - Skip bad patterns
- Change SE
- Use bit counter

No Back Tracing

- BIST
- Test set known

\[ ISD = \sum (\text{IllegalPatterns}) \]

- Larger than back tracing ISD \(\oplus\)
ISD-Counter

- BIST
  - Pattern counter
  - Test Length = \( M \)
  - Pattern Counter size = \( \lceil \log_2(M) \rceil \)

\[ ISD = \sum (CounterValue(IlllegalPatterns)) \]

- Much smaller area 😊

Mapping Logic

- Source patterns = Illegal patterns
- Image patterns = ATPG generated
- Good source patterns
  - Mapped to themselves
  - Otherwise, illegal again

- Only \( n/2^n \) of the patterns are legal
  \( \Rightarrow \) Large mapping area
Benchmarks

<table>
<thead>
<tr>
<th>Circuit Name</th>
<th>Pls</th>
<th>POs</th>
<th>FFs</th>
<th>Area</th>
<th>One Hot</th>
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<td>6</td>
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ISD-Trace

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<th>Area</th>
<th>ISD-Trace ISD-Inputs</th>
<th>Circuit</th>
<th>Area</th>
<th>ISD-Trace ISD-Inputs</th>
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<td>16</td>
<td>C6288</td>
<td>8836</td>
<td>16</td>
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</tbody>
</table>
Why large area “sometimes”?

- Large number of one-hot signals
  - Although circuits are small
- Logic cones are large

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Area</th>
<th>Random Test Length</th>
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<tr>
<td>s400</td>
<td>863</td>
<td>35 56 204</td>
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<tr>
<td>s713</td>
<td>879</td>
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<td>28 60 306</td>
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<td>15 37 104</td>
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ISD-Counter

<table>
<thead>
<tr>
<th>Circuit</th>
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<th>ISD-Counter Area Overhead</th>
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<tr>
<td>s400</td>
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<td>0.07  0.18  0.49</td>
</tr>
</tbody>
</table>

ISD Area vs. Test Length

![Graph showing ISD Area vs. Test Length]

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ISD Area vs. Test Length

Conclusions

- ISD technique generally applicable
  - IC production, board-level and system-level
- No fault coverage sacrifice
- Almost, non-intrusive
- Very low area overhead
- Very low delay overhead
- ISD-Trace and ISD-Counter complement
- Any restriction, not only one-hot
- Combines with test length reduction techniques
References