Motivation

- Pseudorandom Test
  - Effectiveness with real defects
  - Probablistic models
  - Defect and fault coverage (SSF)
  - Defect level estimation and tester data
  - Unmodeled (colateral) coverage
  - Mapping logic effectiveness
Built-In Self-Test

- On-chip circuitry
  - Pattern generation (LFSR)
  - Response compression (MISR)
- Low-cost 😊
- Circuit speed 😊
- Applicability while in system 😊

But ..
- Test length 😞
- Area overhead 😞
- Fault coverage 😞

Pseudorandom Test

- Pseudorandom patterns
  - LFSR
- Test quality
  - Fault coverage
    - SSF
    - Transition faults
Test Chip Experiment

- Compare
  - Actual production defects
  - Fault models

- How
  - Collect
    - Defective chips
    - Test sets
      - Various test metrics
      - Various test conditions

Murphy Chip

- LSI Logic 150K CMOS Gate Array
- 25K Gate design
- $L_{\text{eff}} = 0.7 \ \mu\text{m}$
- Nominal VDD = 5v
- 5 Combinational CUT designs
  - 4 Copies of each CUT
- Support DFT circuitry
ELF35 Chip

- LSI Logic G10P technology
- $L_{\text{eff}} = 0.35 \mu m$
- Nominal VDD = 3.3v
- 6 CUT designs
  - 4 Combinational CUT designs
    - 1 translator, 3 datapath
  - 2 Sequential (2901’s) with full scan

Murphy CUTs Studied

- M12
  - 24 Inputs, 12 Outputs, 1,146 gates
  - $12 \times 12$ multiplier
  - 38 defective M12 CUTs
- ROB
  - 24 Inputs, 12 Outputs, 898 Gates
  - $12 \times 12$ mult. (robust path-delay fault testable)
  - 30 defective ROB CUTs
ELF35 CUTs Studied

- **M12**
  - 24 Inputs, 12 Outputs, 1,309 gates
  - \(12 \times 12\) multiplier
  - 38 defective M12 CUTs

- **PB**
  - 12 Inputs, 12 Outputs, 17,468 Gates
  - Pseudorandom to Binary translator
  - 139 defective PB CUTs

Test Escapes

- Undetected defective CUTs
Fault and Defect Coverage

- **Fault coverage**
  - Fraction of modeled faults detected by test set
  - Estimated theoretically or
  - Computed by simulation

- **Defect coverage**
  - Fraction of defective chips detected
  - On the tester
  - Using the given test set

Fault and Defect Coverage

- **SSF coverage and defect coverage**
  - Any correlation?

- **SSF coverage**
  - Fault simulation

- **Defect coverage**
  - Tester data
Defect and Fault Coverage (Murphy/ROB)

Defect & Fault Coverage (Murphy/M12)
Defect & Fault Coverage (ELF35/M12)

Defect & Fault Coverage (ELF35/PB)
Fault Coverage Estimation

- McCulskey et. al. (IEEE Trans. CAD 88) [1]
  - Relates
    - Pseudorandom test length
    - Fault coverage (SSF)
  - CUT dependence
    - Detectability profile
      - SSF detection characteristics

Fault Coverage Theoretical Estimation

\[ E(C) = 1 - \left( \frac{1}{n_f} \right) \sum h_k e^{\left( -\frac{kL}{N} \right)} \]

- \( E(C) \) = Expected fault coverage
- \( n_f \) = Number of SSFs in the CUT
- \( h_k \) = Number of faults of detectability k
- \( N \) = Total number of different patterns
- \( L \) = Test length
BIST Escapes

- Compare the escapes vs. test length
  - Theoretical model
  - Fault simulation
  - Tester data

Escapes results (Murphy/ROB)

Theoretical - • Tester Data — Simulation
Escapes Results (Murphy/M12)

Test Length vs. Escapes

- Theoretical
- Tester Data
- Simulation

Escapes Results (ELF35/M12)

Test Length vs. Escapes

- Theoretical
- Tester Data
- Simulation
Defect level prediction

- Williams-Brown model
- McCluskey-Buelow model

\[ DL = 1 - Y^{TT} \]

- DL = Defect Level (defect per million)
- Y = Yield
- TT = Test Transparency
Defect Level Calculation

- **TT (Test Transparency)**
  - Estimated by fault uncovery
    - TT = 1 – FC
  - Using Single Stuck at Faults
- **Fault coverage computation**
  - By simulation
  - Using theoretical models
    \[
    Y = 1 - \frac{\text{Number of defective CUTs}}{\text{Total number of CUTs}}
    \]

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Defect Level (Murphy/ROB)

- Theoretical
- Simulation
- Tester data

![Defect Level Graph](image-url)
Defect Level (Murphy/M12)

Defect Level (ELF35/M12)
Defect Level (ELF35/PB)

Theoritical    Simulation    • Tester date

Collateral Coverage

- Detecting unmodeled defects
  - Many
- Non fault-dropping patterns (NFDPs)
  - Patterns that don’t drop new faults

Collateral Coverage = \[\frac{\text{Number of defects detected by NFDPs}}{\text{Total number of defective chips}}\]
## Collateral Coverage

<table>
<thead>
<tr>
<th></th>
<th>Coverage (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Murphy/ROB</td>
<td>16.67%</td>
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<tr>
<td>Murphy/M12</td>
<td>2.63%</td>
</tr>
<tr>
<td>ELF35/M12</td>
<td>5.41%</td>
</tr>
<tr>
<td>ELF35/PB</td>
<td>1.45%</td>
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## Mapping Logic [3]

- Given an LFSR and a test length
- Find a cube with no fault dropping patterns
- Map to an image cube to increase coverage
- Add the additional H/W to the LFSR
Mapping Logic

Original Test Patterns

Pattern Generator

Mapping Logic

Transformed Test Patterns

Circuit Under Test (CUT)

Is it effective in catching defects?

Detects defective chips

Faster or slower?
**Conclusions**

- Fault coverage ≠ Defect coverage
- Fault escapes
  - Theoretical model → Very pessimistic
  - Fault simulation → Still pessimistic
  - Tester data almost always better
- Defect level
  - TT estimated theoretically → Very pessimistic
  - TT obtained by simulation → Still pessimistic
- Collateral coverage → reasonably high
BIG NEWS

- Single stuck fault model
  - NOT ACCURATE
- Pseudorandom testing
  - BETTER THAN IT SEEMS
    - Both by theoretical models and fault simulation
- Mapping logic
  - Catches defects fast

References