Outline

- Introduction
- NAND gate Example
- Diagnosis Flow
- Experimental Results
- Summary

Murphy Test Chip

- 0.7μm technology, 5V nominal VDD
- LSI gate array
- 25K gates, combinational circuits

Sequence Dependence

- Test results
  - Pattern sequence dependent
- Possible cause
  - Stuck-open (SOP) fault [Wasdack 78]
- Goal of this talk
  - Diagnosis
    - ⇒ 11 sequence dependent only chips

Defect Classification

- 116 defective chips (total 5.5K tested)
  - 11 sequence dependent only chips

Previous Work

- Stuck-open fault simulation
  - [Barzilai 86] [Konuk 96]
  - No experimental data
- Interconnect open [Venkataraman 00]
  - Composite Signature
  - No sequence dependence
- General Diagnosis [Hora 01]
  - No fault model
  - No sequence dependence
- Stuck-open fault diagnosis [Li 01]
  - Single fault only

Diagnosis of Sequence Dependent Murphy Chips

James Chien-Mo Li
RATS Seminar
CRC, Stanford University
Oct. 1, 2001
Diagnosis of Sequence Dependent Murphy Chips

Features of This Diagnosis

• Multiple faults
• Two fault models
  • Single Stuck-at Fault (SSF)
  • Stuck-open fault
• Real experimental data

Outline

• Introduction
• NAND gate Example
• Diagnosis Flow
• Experimental Results
• Summary

Stuck-open (SOP) Fault

• 4 faults in NAND

Sequence Dependence

• Stuck-open fault T1
  • AB=00,11,01 -> detected
  • AB=00,01,11 -> not detected

Excitation Condition (EC)

• Pair of gate inputs
  • Excite SOP fault
• Example
  • SOP fault T1

EC Table

• All SOP faults
• NAND Example

<table>
<thead>
<tr>
<th>Pattern#</th>
<th>A</th>
<th>B</th>
<th>Detected fault</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>T1</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>1</td>
<td>T3,T4</td>
<td></td>
</tr>
</tbody>
</table>

EC Table for NAND

<table>
<thead>
<tr>
<th>A*</th>
<th>B</th>
<th>Detected fault</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>F</td>
<td>S1</td>
<td>T1</td>
<td>R</td>
</tr>
<tr>
<td>S1</td>
<td>F</td>
<td>T2</td>
<td>R</td>
</tr>
<tr>
<td>R</td>
<td>S1</td>
<td>T3,T4</td>
<td>F</td>
</tr>
<tr>
<td>S1</td>
<td>R</td>
<td>T3,T4</td>
<td>F</td>
</tr>
</tbody>
</table>

F = Fall, R = Rise, S1=Static 1
Diagnosis of Sequence Dependent Murphy Chips

Outline

• Introduction
• NAND gate Example
• Diagnosis Flow
  • Diagnosis Terminology
  • Step-by-step descriptions
• Experimental Results
• Summary

Diagnosis Terminology

• Fault Signatures (FS)
  • Predicted by fault simulation
    ➔ Failing patterns
    ➔ Failing pins
• Failure Trace (FT)
  • Observed from tester
    ➔ Failing patterns
    ➔ Failing pins

Diagnosis Terminology (2)

• Intersection (I)
  • Both observed and predicted
• Simulation only (SO)
  • Predicted but not observed
• Tester only (TO)
  • Observed but not predicted

Overall Diagnosis Flow

Test ➔ Failure Trace
SSF Diagnosis ➔ Diagnosed SSF faults
SSF Fault Sim. ➔ Fault signatures (SSF)
Post Processing ➔ Fault signatures (SOP)
Match ➔ Diagnosed faults

STEP 1. Collect Data on Tester

• Failure trace observed
• Example: NAND gate with SOP fault T1

<table>
<thead>
<tr>
<th>Failing pattern</th>
<th>Failing pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>PO1</td>
</tr>
<tr>
<td>N</td>
<td>PO2</td>
</tr>
</tbody>
</table>
Diagnosis of Sequence Dependent Murphy Chips

STEP 2. SSF Diagnosis
- Commercial tool
- Diagnosed stuck-at faults obtained
- NAND Example (cont’d)
  - A s@1 diagnosed

STEP 3. Stuck-at Fault Simulation
- Commercial tool
- Fault signatures obtained
- NAND example (cont’d)
  - A stuck-at 1 fault (from STEP 2.)

<table>
<thead>
<tr>
<th>FS for A s@1</th>
<th>Pattern</th>
<th>Falling pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>1</td>
<td>PO1</td>
</tr>
<tr>
<td>M</td>
<td>1</td>
<td>PO2</td>
</tr>
<tr>
<td>N</td>
<td>1</td>
<td>PO2</td>
</tr>
</tbody>
</table>

STEP 4. Logic Simulation
- All tester patterns simulated (fault free)
  - Gate Input Sequence (GIS) Table obtained
- NAND example (cont’d)

GIS Table

```
Pattern | A | B | 2
-------|---|---|---
L-1     | 1 | 0 | 0
L       | 0 | 1 | 1
M       | 0 | 0 | 1
M-1     | 0 | 1 | 1
M-1     | 1 | 1 | 0
N-1     | 0 | 1 | 1
M       | 0 | 1 | 1
(last)  |   |   |   
```

STEP 5. Post Processing
- Create FS for SOP faults
  - From FS for SSF
- How?
  - For every FS in SSF
    - Check previous gate inputs

Overall Diagnosis Flow

Overall Diagnosis Flow

Overall Diagnosis Flow
**NAND Example**

- SOP fault T1
  - Excited by pattern [L-1, L] (see EC table)
  - Propagation implied by SSF simulation

<table>
<thead>
<tr>
<th>Pattern</th>
<th>A</th>
<th>B</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>L-1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>L</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>M-1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>M</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>N-2</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>N-1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>N</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

![EC Table for NAND](image)

**NAND Example (cont’d)**

- N-1 identical to N
  - Check N-2

<table>
<thead>
<tr>
<th>Pattern</th>
<th>A</th>
<th>B</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>L-1</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>L</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>M-1</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>M</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>N-2</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>N-1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>N</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

**STEP 5. Results**

- FS for SOP fault obtained
- NAND example (cont’d)

**FS for SOP fault T1**

<table>
<thead>
<tr>
<th>Failing pattern</th>
<th>Failing pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>PO1</td>
</tr>
<tr>
<td>N</td>
<td>PO2</td>
</tr>
</tbody>
</table>

**STEP 6. Match [Hora 01]**

**Overall Diagnosis Flow**

- Test
- Failure Trace
- SSF Diagnosis
- Diagnosed SSF faults
- SSF Fault Sim.
- Fault Signatures (SSF)
- Post Processing
- Fault Signatures (SOP)
- Match
- Diagnosed faults

**Diagnosis of Sequence Dependent Murphy Chips**

James Chien-Mo Li

Page 5

Monday, Oct. 1, 2001
Diagnosis of Sequence Dependent Murphy Chips

4 Matching Outcomes

- Case A: M=P = 100
  - Perfect match
- Case B: P=100, M<100
  - All FS actually observed
  - Some FT not predicted
  - Example: multiple stuck-at or SOP faults

 FS FT  FS FT
Case (A) P=100, M=100 Case (B) P=100, M<100

4 Matching Outcomes

- Case C: M=100, P<100
  - All FT predicted
  - Some FS not observed
  - Example: bridging
- Case D: M<100, P<100
  - Not interesting

 FS FT  FS FT
Case (C) M=100, P<100 Case (D) P<100, M<100

STEP 6. Matching

- NAND example (cont'd)
  - FS = FT
  - Perfect match

 FT
Failing pattern Failing pin
L PO1
N PO2

FS for SOP fault T1
Failing pattern Failing pin
L PO1
N PO2

No Perfect Match

- Multiple faults selection
  - Pick faults
  - P=100, highest M score
- Example
  - Pick Fault 1, then fault 2, then fault 3

 FS Fault 1 FT
FS Fault 2
FS Fault 3

Outline

- Introduction
- NAND gate Example
- Diagnosis Flow
- Experimental Results
- Summary

Experiment Setup

- 11 sequence dependent Murphy chips
- 15 detect SSF test set
- Scan out primary outputs
  - Failing patterns
  - Failing pins
- Max 255 failures observable
  - Tester limitation
Diagnosis of Sequence Dependent Murphy Chips

Chips #1-5
- Single SOP fault diagnosed
- Perfect Match

<table>
<thead>
<tr>
<th>Chip ID</th>
<th>SSF diagnosis</th>
<th>Stuck-open diagnosis</th>
<th># of faults</th>
<th>Score M/P</th>
<th>Faulty gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>3</td>
<td>100/100</td>
<td>NOR</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>1</td>
<td>100/100</td>
<td>NOR</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>1</td>
<td>100/100</td>
<td>AOI</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td>4</td>
<td>100/100</td>
<td>OR</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td>4</td>
<td>100/100</td>
<td>AOI</td>
</tr>
</tbody>
</table>

Chip #6-7
- P=100, M<100
- Tester only failure trace
- Example: NAND with SOP fault T1
  - AB = (11,01)
    - Fail, as predicted
  - AB = (10,01)
    - Also fail, why?

Timing Skew [Reddy 84]
- Uncertainty of relative timing
  - Two signals change values
- NAND example (cont’d)
  - AB = (10,01)
    - Case A: A falls then B rises
    - Case B: B rises then A falls

Timing Skew
- Different test results
  - Case A: open not detected
  - Case B: open could be detected

Chip #6-7
- Adding double input changes
  - AB = (01,10) to EC table
- Perfect match
- Better diagnosis resolution
  - Commercial SSF diagnosis

<table>
<thead>
<tr>
<th>Chip ID</th>
<th>SSF diagnosis</th>
<th>Stuck-open fault diagnosis (modified EC table)</th>
<th># of faults</th>
<th>Score M/P</th>
<th>Faulty gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td></td>
<td></td>
<td>40</td>
<td>100/100</td>
<td>NAND</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>10</td>
<td>100/100</td>
<td>OAI</td>
</tr>
</tbody>
</table>

Chip #8-9
- Similar timing skew problem
  - Modified EC table
- Multiple faults
  - A big defect? Multiple defects?

<table>
<thead>
<tr>
<th>Chip ID</th>
<th>SSF diagnosis</th>
<th>Stuck-open fault diagnosis (modified EC table)</th>
<th># of faults</th>
<th>Score M/P</th>
<th>Faulty gate</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>37</td>
<td>200/100</td>
<td>NAND (SSF)</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td>20</td>
<td>200/100</td>
<td>NAND (SSF)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>OAI (SSF)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>OAI (SOP)</td>
</tr>
</tbody>
</table>
Diagnosis of Sequence Dependent Murphy Chips

Chip #10-11
- Faulty gate: MUX
- M score =100, P<100
- Input pin & output pin
- Case (C) in STEP 6

Summary of 11 Murphy Chips

<table>
<thead>
<tr>
<th>Chip ID</th>
<th>Perfect match?</th>
<th>Diagnosed faults</th>
</tr>
</thead>
<tbody>
<tr>
<td>1-7</td>
<td>Y</td>
<td>1 SOP fault</td>
</tr>
<tr>
<td>8</td>
<td>Y</td>
<td>1 SSF + 1 SOP</td>
</tr>
<tr>
<td>9</td>
<td>N</td>
<td>2 SSF + 1 SOP</td>
</tr>
<tr>
<td>10,11</td>
<td>N</td>
<td>unknown</td>
</tr>
</tbody>
</table>

Summary
- Diagnosis technique
  - Stuck-at, stuck-open faults
  - Multiple faults
- Experimental Results

References