Diagnosis of Sequence Dependent Chips

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James C.M. Li and Edward J. McCluskey
CRC, Stanford University

Outline

- Introduction
- Diagnosis Flow
- Experimental Results
- Summary

Sequence Dependence (SD)

- Tester response depends on pattern sequence
- Example:

<table>
<thead>
<tr>
<th>I1</th>
<th>I2</th>
<th>I3</th>
<th>I4</th>
<th>I5</th>
<th>I6</th>
<th>O1</th>
<th>O2</th>
<th>O3</th>
<th>O4</th>
<th>O5</th>
<th>O6</th>
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</thead>
<tbody>
<tr>
<td>Comb. Circuit</td>
<td></td>
<td></td>
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<tr>
<td>O1, O2, O3, O4, O5, O6</td>
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Combinational

<table>
<thead>
<tr>
<th>I6</th>
<th>I5</th>
<th>I4</th>
<th>I3</th>
<th>I2</th>
<th>I1</th>
<th>O6</th>
<th>O5</th>
<th>O4</th>
<th>O3</th>
<th>O2</th>
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Sequence dependent

<table>
<thead>
<tr>
<th>I6</th>
<th>I5</th>
<th>I4</th>
<th>I3</th>
<th>I2</th>
<th>I1</th>
<th>O6</th>
<th>O5</th>
<th>O4</th>
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Other reordered sequence possible

Possible Causes for SD

- Single Stuck-at Fault (SSF)?
  - No
- Feedback bridging fault?
  - Possible
  - Diagnosis difficult
    - Layout information unavailable
- Stuck-Open Fault (SOF)?
  - Possible
  - Diagnosis possible
  - Schematic available in databook

Diagnosis of SD Chips

- Murphy experiment [McCluskey ITC’00]
  - 116 defective chips (total 5.5K tested)
    - 11 SD chips (Test speed independent)
      - Focus of this research
    - 39 SD chips (Test speed dependent)
      - One resistive open [Li ITC’01]
      - Still working on others
- Goal of this research
  - Identify cause of 11 SD chips
  - Locate failure site

Stuck-Open Fault (SOF) Model

- Proposed by Wasdack in 78
  - Transistor fails to turn on
- Example: NAND
  - 4 Stuck-open fault sites: T1..4

B        T1
A          T2
T3       T3
T4       T4
Z
Diagnosis of Sequence Dependent Chips

SD Caused by Stuck-open Fault
- NAND example: T1 stuck-open fault
  - Seq. 1: detected
  - Seq. 2: undetected
  - Charges stored in Z

<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>Zgood</th>
<th>Z1_SOF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Seq. 1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Seq. 2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
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</table>

Previous Related Work
- Stuck open fault simulation [Barzilai 86] [Konuk 96]
  - Fault simulation only, no diagnosis
  - No experiment
- Transition fault simulation [Waicukauski 87]
  - Fault simulation only, no diagnosis
  - No experiment
- Open diagnosis [Hora 01] [Venkataraman 00]
  - Sequence dependence not considered

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Diagnosis Terminology
- Failure Traces
  - Observed from tester
    - Failing patterns, pins (for test set applied)
- Fault simulation
  - Logic simulation with fault injected
- Fault signatures
  - From fault simulation
    - Failing patterns, pins (for test set simulated)

Diagnosis Flow
- Test Set
- Test
  - Failure Traces (FT)
- SSF Fault Simulation
  - Fault Signatures (SSF)
- Signature Converter
  - Fault Signatures (SOF)
- Matching
- Diagnosis results

Example Circuit
- PI = primary input
- PO = primary output
- CL = combinational logic

Charges stored in Z
A
B
Z
T1
1100
0
1
1
0
0011
Z
T1_SOF
0011
1
1
1
0
1100
Z
T1_SOF
19
52
Diagnosis of Sequence Dependent Chips

Diagnosis of Example Circuit
- Test
  - Failure traces
- SSF fault simulation
  - FS for A/1
- Signature Converter
  - FS for T1 SOF
- Match FT with FS
  - T1 SOF diagnosed

Signature Converter
- Why?
  - Convert SSF signatures to SOF signatures
- How?
  - For every failing pattern J in SSF signature
    - Check pattern pair \( \{J-1, J\} \)
    - SOF excited?
      - Yes, SSF signature J \( \Rightarrow \) SOF signature
      - No, SSF signature J discarded

Excitation Condition Table
- Gate input pairs excite SOF
- NAND example

Signature Conversion Example
- Pattern J,K both detect A/1 (SSF simulation)
  - \( \{J-1, J\} \) excite T1 SOF
  - \( \{K-1, K\} \) no excitation

Signature Conversion Example (2)
- Pattern J
  - T1 SOF excited by \( \{J-1, J\} \)
  - Propagation guaranteed by SSF simulation
    - T1 SOF detected
    - SSF signature copied
- Pattern K
  - T1 SOF not excited by \( \{K-1, K\} \)
  - T1 SOF not detected
  - SSF Signature discarded

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The “Murphy Test Chip”
- Test chip description [McCluskey ITC’00]
  - 0.7µm technology, 5V nominal VDD
  - 25K gates, combinational circuits
  - 5 designs: 2 data path, 3 control Logic
  - 5.5K chips tested
  - 11 sequence dependent chips
    - Speed independent
    - SD.1 to SD.11

Diagnosis Results (SD.1 to 7)
- 15 detect SSF test set applied
  - Other test sets in paper

<table>
<thead>
<tr>
<th>Chip ID</th>
<th>SSF diagnosis</th>
<th>SOF diagnosis</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># of faults</td>
<td># of faults</td>
</tr>
<tr>
<td>SD.1</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>SD.2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SD.3</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>SD.4</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>SD.5</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SD.6</td>
<td>40</td>
<td>1</td>
</tr>
<tr>
<td>SD.7</td>
<td>10</td>
<td>1</td>
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</table>

SD.8 and SD.9
- Single fault diagnosis failed
  - Neither SSF nor SOF
  - Combination of two fault signatures
    - Match failure traces
  - Example
    - Fault Signature (X/1 SSF)
    - Fault Signature (TY SOF)

Improved Diagnosis Flow
- Test Set
  - Test
  - SSF Fault Simulation
    - Fault Signatures (SSF)
  - Signature Converter
    - Fault Signatures (SOF)
  - Matching
    - Failure Traces
  - Diagnosis results

Diagnosis Results (SD.8, 9)
- Multiple faults diagnosed
  - Present simultaneously

<table>
<thead>
<tr>
<th>Chip ID</th>
<th>Commercial SSF diagnosis</th>
<th>SOF + SSF diagnosis</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># of faults</td>
<td>Faulty gate</td>
</tr>
<tr>
<td>SD.8</td>
<td>37</td>
<td>2</td>
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<tr>
<td>SD.9</td>
<td>20</td>
<td>3</td>
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Possible Reason for Multiple Faults
- Clustered defects

Wafer map
Unsuccessful Diagnosis (SD.10,11)
- Possible reasons
  - Feedback bridging faults
  - Mismatch of library elements
    - Schematic shown in book
    - Actual implementation

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Summary
- Diagnosis technique presented
  - Multiple faults
  - 2 fault models
    - SSF, SOF
- Demonstrated by experiment
  - 11 sequence dependent chips
    - 7 chips: single stuck open fault
    - 2 chips: multiple faults (SSF + SOF)

Thank You!