Some Suggestions
From the Murphy-Elf Tester Data
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Experiment Purpose
- Compare
  - Actual Production Defects
  - Fault Models
- How?
  - Collect
    - Defective Chips
    - Test Sets
      - various test metrics
      - various test conditions

Discoveries
- Defective chip characteristics
- Defective chip test responses
- Defective chip test set dependence
- New test metrics
  - N-detect, TARO
- Defective chip test coverage dependence
- Few defects cause test escapes
- VLV slow speed testing
- Some Diagnosis results

Discoveries
- Few defects act like single-stuck faults
  - Murphy – 35%, ELF – 1%
- Many defects cause sequence dependence
  - Murphy – 43%, ELF – 58%
- Some defects cause timing dependence
  - Murphy – 34%, ELF – 31%

Defect Tester Characteristics
Murphy

<table>
<thead>
<tr>
<th>TIC-SSF (41)</th>
<th>TIC-nonSSF (25)</th>
<th>Sequence &amp; Timing Dependent (39)</th>
<th>Sequence Dependent only (11)</th>
</tr>
</thead>
<tbody>
<tr>
<td>35%</td>
<td>22%</td>
<td>34%</td>
<td>9%</td>
</tr>
</tbody>
</table>

Total 116 defective chips

ELF35

<table>
<thead>
<tr>
<th>TIC-SSF (5)</th>
<th>Sequence &amp; Timing Dependent (107)</th>
</tr>
</thead>
<tbody>
<tr>
<td>31%</td>
<td></td>
</tr>
</tbody>
</table>

Total 343 defective chips

Sequence Dependent
Tester response depends on pattern sequence

combinational

Sequence dependent

Sequence dependent escape

Diagram showing test response patterns and outcomes.
Chip Test Set Reordering

- all-zero vector
  - inserted between all patterns,
- all-one vector
  - inserted between all patterns,
- Bit-wise complements
- One bit shift
- Reverse sequence

Timing Dependent

Tester response depends on pattern timing

Hard Defect Classification - Diagnosis

- Timing dependent
  - Tester response depends on test speed
- Sequence dependent
  - Tester response depends on pattern sequence
- TIC (Timing independent combinational)
  - Neither sequence nor timing dependent
  - SSF match
  - Tester response matches SSF simulation

Hard Defect Classification - Test

- Sequence Dependent Escape (SDE)
  - Pass/fail result depends on pattern sequence
- Sequence and Timing Dependent Escape (STDE)
  - Pass/fail result depends on both sequence and speed
- Solid Defect
  - Fails at all test sequences and speeds

Discoveries

- Most defective chips are solid tester fails
  - Fail at all tester speeds and test sequences
    - Murphy – 81% (95 / 116), ELF – 98% (337 / 343)
- Few defective chips
  - Fail for only some test sequences
    - Murphy – 19% (21 / 116), ELF – 2% (5 / 343)
  - Fail at only some test speeds
    - Murphy – 3% (3 / 116), ELF – 0.3% (1 / 343)

Murphy

- STDE (3)
- SOLID (95) 81%

ELF35

- STDE (1)
- SOLID (337) 98.5%
Discoveries
• Most defective chips fail all test sets
  - Murphy – 62%, ELF – 82%
• Few defective chips
  - Fail at only some test sequences
  - Murphy – 19%, ELF – 2%
  - Fail at only some test speeds
  - Murphy – 3%, ELF – 0.3%

Observations
• Tester results depend on the test set
• Some test set metrics are more effective

Test Set Metrics
• Design Verification
• Toggle
• Single-stuck Fault
• Multiple-stuck Fault
• N-detect Single-stuck Fault
• Bridging Fault
• Transition Fault
• Delay Fault: Gate, Path
• TARO

New Metrics
• N-detect
  • Each SSF detected by
  • N Different Test Patterns
• TARO
  • Transition fault sensitized to
  • All Reachable Outputs
  • More thorough than transition faults
  • Fewer patterns than complete path delay
  • More effective than longest paths

Chip Package Test
• Tester
  • Advantest T6671E VLSI Test System
  • 125MHz clock rate
Murphy Chip Package Test

Test Time: 10 minutes per chip on average
- 5 minutes per good chip
- 20 minutes per interesting chip
- 10 minutes average
* 309 dies packaged (5,491 dies probed)
* 10 weak suspects
* 116 defective chips
- 73 fail all test sets -- FATS
- 43 fail only some test sets -- FOSTS

ELF35 Chip Package Test

Test Time:
- 2 minutes per good chip
- 20 minutes per interesting chip
* 9,566 chips packaged and tested
* 343 defective chips,
- 280 fail all test sets -- FATS
- 63 fail only some test sets -- FOSTS
* 171 weak suspects

Murphy Chip Test Sets

* 265 test sets
- 162 single stuck fault based
- 55 delay fault
  - 8 gate delay fault
  - 32 path delay fault
  - 10 transition fault
  - 5 stuck-open fault
- 10 weighted random
- 2 design verification vectors
- 30 IDDQ
- 5 exhaustive, 1 super exhaustive

ELF35 Chip Test Sets

* 278 test sets
- 140 single stuck fault based
- 78 delay fault
  - 58 Path delay fault
  - 20 Transition fault
- 4 weighted random
- 6 design verification vectors
- 6 toggle
- 32 IDDQ
- 6 exhaustive, 1 super exhaustive
- 5 BIST
Test Results for 13 Solid Escape Murphy Chips

Test Results for 14 Dependent Escape Murphy Chips

Observations

- Few timing defects cause test escapes
- Of all defects
  - Murphy – 3% (3 / 116), ELF – 0.3% (1 / 343)
- Of all timing defects
  - Murphy – 6% (3 / 39), ELF – 1% (1 / 107)
- Slow speed VLV test can be effective

VLV for Reliability Defects or Flaws

- Lower \( V_{DD} \)
- Between 2 and 2.5 normal \( V_T \)
  - Scaled speed
- Apply test patterns
  - Discard failing chips

VLV Voltage

- Murphy
  - \( NV = 5V \)
  - \( VLV = 1.7V \)
  - \( V_T = 0.85V \)
- ELF35
  - \( NV = 3.3V \)
  - \( VLV = 1.4V \)
  - \( V_T = 0.7V \)

Nominal Voltage Testing Results

- Murphy
  - At-Speed: 116 Defective Chips
  - Slow Speed: 113 Defective Chips
    - 3 Slow Escapes
- ELF35
  - At-Speed: 218 Defective Chips
  - Slow Speed: 217 Defective Chips
    - 1 Slow Escape

How can we do better??
Why VLV Testing?

- Defects
  - Accelerated by Lower Voltage
  - NV Test Escapes
  - Hard Failures
  - Timing Failures
- Slow Speed
  - Scaled Speed @ VLV
  - Much Slower than Characterized Speed
- Power
  - Less Power Consumption at VLV
    \[ P = fCV^2 \]

Murphy Test Results

5,491 dies tested

NV Boolean Failures

VLV Boolean Failures

VLV IDDQ Failures (3uA)

Test Speed Questions

- What if we test?
  - At normal voltage, characterized speed?
  - At normal voltage, slow speed?
  - At reduced voltage (VLV), scaled speed?
  - At reduced voltage (VLV), slow speed?

ELF35 Test Results

9,566 chips tested

NV Boolean Failures

VLV Boolean Failures

VLV IDDQ Failures (100uA)

Terminology

- Characterized Speed
  - Chip Speed at Nominal Supply Voltage (NV)
- Scaled Speed
  - Chip Speed at Other Supply Voltages
  - Function of Voltages
- Slow Speed Testing
  - Test Speed
    - 1/3 Characterized Speed (Test @ NV)
    - Or
    - 1/3 Scaled Speed (Test @ Other Voltages)

VLV Testing: Speed and Power

- Scaled Speed @ VLV
  - 4X-5X Slower
- Power
  - 3% @ VLV (Murphy)
Terminology

- **Murphy Chips**
  - Characterized Speed (5V): 26ns
  - Scaled Speed (1.7V): 130ns

![Supply Voltage VDD (V) vs. Clock Cycle Time (ns)](image)

Murphy VLV Testing Results

- 3 NV Slow Speed Escapes
  - Chip1
    - NV: 10% Slow (Escape Slow Speed Testing)
    - VLV: Hard Failure
  - Chip2
    - NV: 15% Slow (Escape Slow Speed Testing)
    - VLV: Hard Failure
  - Chip3
    - Escaped VLV Testing at 70% Scaled Speed

Murphy Chip Results

<table>
<thead>
<tr>
<th>Test Conditions</th>
<th>Test Voltage</th>
<th>Test Speed</th>
<th>Escapes</th>
</tr>
</thead>
<tbody>
<tr>
<td>NV, At-Speed</td>
<td>5</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>NV, Slow Speed</td>
<td>0.33</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>VLV, Scaled-Speed</td>
<td>1.7</td>
<td>0.25</td>
<td>0</td>
</tr>
<tr>
<td>VLV, Slow Speed</td>
<td>0.08</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

- **VLV Testing**
  - Scaled-speed Testing
    - As Effective as NV at-speed Testing
  - Slow Speed Testing
    - Better than NV Slow Speed Testing

ELF35 VLV Testing Results

- VLV Scales Speed
- VLV 80% Scales Speed
- VLV 70% Scales Speed
- VLV Slow Speed

ELF35 Chip Results

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<th>Test Conditions</th>
<th>Test Voltage</th>
<th>Test Speed</th>
<th>Escapes</th>
</tr>
</thead>
<tbody>
<tr>
<td>NV, At-Speed</td>
<td>3.3</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>NV, Slow Speed</td>
<td>0.33</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>VLV, Scaled-Speed</td>
<td>1.4</td>
<td>0.20</td>
<td>0</td>
</tr>
<tr>
<td>VLV, Slow Speed</td>
<td>0.06</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

- **VLV Testing**
  - Scaled-speed Testing
    - As Effective as NV at-speed Testing
  - Slow Speed Testing
    - As Effective as NV Slow Speed Testing
Other Questions

• Diagnosis?

Murphy Diagnosis

• 116 defective chips (43 FOSTS, 73 FATS)
  - 66 TIC (20 FOSTS, 46 FATS)
  - 41 SSF diagnosed (14 FOSTS, 27 FATS)
  - 25 non-SSF (6 FOSTS, 19 FATS)
  - 50 non-TIC (23 FOSTS, 27 FATS)
  - 11 Sequence Dependent (6 FOSTS, 5 FATS)
    - 7 single stuck-open diagnosed
    - 2 multiple faults diagnosed
  - 39 Sequence and Timing Dependent
    - 17 FOSTS, 22 FATS
    - 1 resistive open diagnosed
• 9 VLV-only failure
  - 5 tunneling open diagnosed

Murphy Diagnosis

All Boolean Failures at Nominal Voltage

- 116
- 66
- 50
- 41 SSF diagnosed
- 25
- 11 Sequence Dependent
- 39 Non-TIC
- 7 stuck-open
- 2 multiple faults
- 1 resistive open diagnosed

Stuck-open Diagnosis [Li VTS’02]

• 7 stuck-open suspect chips diagnosed
  - More precise results than commercial tool

<table>
<thead>
<tr>
<th>Chip ID</th>
<th>Commercial SSF diagnosis</th>
<th>Our diagnosis</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># of faults</td>
<td># of faults</td>
</tr>
<tr>
<td>SD.1</td>
<td>3</td>
<td>1</td>
</tr>
<tr>
<td>SD.2</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SD.3</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>SD.4</td>
<td>4</td>
<td>1</td>
</tr>
<tr>
<td>SD.5</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>SD.6</td>
<td>40</td>
<td>1</td>
</tr>
<tr>
<td>SD.7</td>
<td>10</td>
<td>1</td>
</tr>
</tbody>
</table>

* not perfect match

Stuck-open Diagnosis (cont’d)

• 2 Multiple faults diagnosed
  - Present simultaneously

<table>
<thead>
<tr>
<th>Chip ID</th>
<th>Commercial SSF diagnosis</th>
<th>SOF + SSF diagnosis</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td># of faults</td>
<td>Faulty gate</td>
</tr>
<tr>
<td>SD.8</td>
<td>37</td>
<td>NAND (SSF) OR (SOF)</td>
</tr>
<tr>
<td>SD.9</td>
<td>20</td>
<td>NAND (SSF) OAI (SSF) OR (SOF)</td>
</tr>
</tbody>
</table>

Discoveries

• Defective chip characteristics
• Defective chip test responses
• Defective chip test set dependence
• New test metrics
  - N-detect, TARO
• Defective chip test coverage dependence
• Few defects cause test escapes
• VLV speed testing
• Some Diagnosis results
Acknowledgments

- LSI Logic
- Advantest
- Semiconductor Research Corporation
- Intel
- Agilent
- DTS
- Hughes Aircraft Corporation

Murphy Chip

- LSI Logic 150k CMOS Gate Array
  - (with Crosscheck™ embedded array)
- 25k gate design
- 120-pin Ceramic PGA package
  - 96 signal pins
- $L_{\text{eff}} = 0.7 \mu m$
- Normal VDD = 5 V

Murphy Chip

- Special purpose chip design
  - 5 different combinational circuit designs
    - 3 control logic designs
    - 2 data path designs
    - 4 copies of each CUT
  - Support (DFT) circuitry

MURPHY Time Line

- 1991 Project started
- 1993 Design completed
- 1995 Wafer sort results, ITC
- 1997 Package chips received
- 1998 Package test results, VTS
- 2000 Burn-in results, ITC

ELF 35 Chip

- LSI Logic G10P technology
- $L_{\text{eff}} = 0.35 \mu m$
- 264k gates
- 272-pin Plastic BGA package
- 3.3V Normal VDD
- 6 CUT designs
  - 2 sequential (2901’s) with full scan
  - 4 combinational
    - 1 translator, 3 data path

ELF35 Time Line

- Jan. 1996
- Nov. 1996
- Apr. 1997
- 1998
- 1999
- Nov. 2000
- Aug. 2001
- Mar. 2002

- Project started
- Logic Design Completed
- Tape-out
- First silicon
- Test Patterns Collected
- Test Program Debug
- 3,000+ chips received
- 6,000+ chips received
- All chips tested, ITC paper submitted
ELF 13 Chip

- LSI Logic G-flex technology
- \( L_{\text{eff}} = 0.13 \mu m \)
- 4 million gates
- 400-600 pins
- 5 CUT designs
- 200 MHz

ELF13 status

<table>
<thead>
<tr>
<th>CUT</th>
<th>Building Block</th>
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</thead>
<tbody>
<tr>
<td>Divider</td>
<td>Being laid out</td>
</tr>
<tr>
<td>PB</td>
<td>Ready to be laid out</td>
</tr>
<tr>
<td>BMATCH</td>
<td>Ready to be laid out</td>
</tr>
<tr>
<td>Frame processor</td>
<td>Netlist in progress</td>
</tr>
<tr>
<td>SONET</td>
<td>Ready to be laid out</td>
</tr>
</tbody>
</table>

DOTS