ELF13 Design Overview
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Outline
• ELF13 Chip Design
• CUT Status
• Test Plan
• Tasks

ELF13 Chip Overview
• LSI G-flex 0.13 µm
• 8 layers interconnect
• Speed: 200 MHz (tester max speed)
• 5 Building Blocks
  - PB, DIV
  - BMATCH, SONET, FrameProcessor (FP)
• Die size: 6.5 x 6.5 mm
• Gate Count: 4M gates
• I/O pin: around 450 pins (estimate)
  - reduced SONET, original FP

Gate Count
<table>
<thead>
<tr>
<th>Building Block</th>
<th>CUT Gate Count</th>
<th># of CUTs</th>
<th>Building Block Gate Count</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB</td>
<td>125K</td>
<td>6</td>
<td>750K</td>
</tr>
<tr>
<td>Divider</td>
<td>125K</td>
<td>6</td>
<td>750K</td>
</tr>
<tr>
<td>Bmatch</td>
<td>110K</td>
<td>6</td>
<td>660K</td>
</tr>
<tr>
<td>SONET</td>
<td>127K</td>
<td>6</td>
<td>762K</td>
</tr>
<tr>
<td>Frame</td>
<td>17K*</td>
<td>16</td>
<td>272K</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td></td>
<td>3.2M</td>
</tr>
</tbody>
</table>

* TBD: to be updated
* Total support circuitry: 0.24M

Combinational Circuit Building Block

Input LFSR SI
Output LFSR SO
Error indicator
PO Error indicator
CUT copy #1
CUT copy #2
...
Sequential Circuit Building Block

Scan Chain Estimate

• Assumption: 1000 FFs per chain

<table>
<thead>
<tr>
<th></th>
<th># of FFs</th>
<th># of scan chains</th>
</tr>
</thead>
<tbody>
<tr>
<td>BMATCH</td>
<td>4.5K</td>
<td>5</td>
</tr>
<tr>
<td>SONET</td>
<td>8.7K</td>
<td>9</td>
</tr>
<tr>
<td>FP</td>
<td>925</td>
<td>1</td>
</tr>
<tr>
<td>Support</td>
<td>5.7K</td>
<td>10</td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>25</td>
</tr>
</tbody>
</table>

• Meet tester constrains
  - 64 scan pins (32 chains)

CUT I/O Pin Count

<table>
<thead>
<tr>
<th></th>
<th>Input</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>PB</td>
<td>24</td>
<td>24</td>
</tr>
<tr>
<td>Divider</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>BMATCH</td>
<td>19</td>
<td>88</td>
</tr>
<tr>
<td>SONET</td>
<td>(orig. 329)</td>
<td>(orig. 68)</td>
</tr>
<tr>
<td>FP</td>
<td>(can be reduced to 79)</td>
<td>192</td>
</tr>
</tbody>
</table>

Support Circuitry

• Input LFSR
  - Hold inputs from tester
  - Apply pseudo random (PR) exhaustive tests to CUT
• Output LFSR
  - Capture CUT outputs
  - Apply PR tests for TRC
• Two Rail Checker (TRC)
  - Comparator

Two-rail Checker

• Outputs compliment iff
  - Inputs compliment

A1 & + A2B1 + A2B2

B1 & + A2B1 + A1B2

Two-rail Checker

• Benefits
  - Self-checking
  - Single fault
    - Correct output or non-complement output
  - Can save number of pins
  - Small overhead
• Implementation
  - Tree structure
**Outline**

- ELF13 Chip Architecture
- CUT Status
- Test Plan
- Tasks

**CUT Status (1)**

- PB (24 inputs, 24 output)
  - Synthesized, 7K SSF patterns, 100% coverage
- Divider (20 bits inputs, 20 bits output)
  - Synthesized, 16K SSF patterns, 100% coverage
- Bmatch (19 inputs, 88 output)
  - Synthesized
  - 4.5K FFs, 1 scan chain stitched (can be split)
  - 518 SSF patterns, 99.96% coverage
  - Design verification patterns graded (40 hrs)
  - 33K clock cycles, 99.2% SSF coverage

**CUT Status (2)**

- SONET (329 inputs, can be reduced to 166) (68 outputs, can be reduced to 57)
  - Synthesized, 8.7K FFs, 2 scan chain stitched
  - 3740 SSF patterns, 99.9% coverage
  - 1 functional test case graded (30 hrs)
  - 36K cycles, 20.4%
  - More test cases to grade
- Frame Processor (127 inputs, 192 outputs)
  - Synthesized, 925 FFs, 2 scan chains
  - 1.3K SSF patterns, 99.9% coverage
  - Pin to be reduced
  - Circuit size to be increased

**Chip Integration Status**

- PB, DIV building block
  - Verilog netlist done
  - Input LFSR primitive polynomial
    - $x^{24}+x^{7}+x^2+x+1$
    - $x^{20}+x^3+1$
  - Verification completed
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Test Flow
- 2-stage testing
  - Wafers
  - Package
  - Wafer sort
  - Final package test
  - Support circuitry fail
  - Good chips
  - Interesting Chips

Wafer Sort
- Follow LSI test methodology
  - Contact
  - Gross IDD
  - VIH/VIL, VOH/VOL, IIH/IIL
  - IDDQ
  - Procmon test
- Plus support circuitry tests

Support Circuitry Tests
- VERY thoroughly before testing CUTs
- Testing input/output LFSR
  - Design verification tests
  - ATPG
    - SSF test sets
    - Transition fault test sets
  - Scan chain tests [Makar 96]
  - IDDQ testing

Support Circuitry Tests (2)
- Testing TRC
  - ATPG SSF Test sets
  - Pseudo random tests
    - Generated by output LFSR
    - At-speed testing
    - IDDQ testing

Scan Data Volume Estimate
- 100% SSF test set
  - BMATCH: 4.5K FFs, 518 scan load, 2.3 M bits
  - SONET: 8.7K FFs, 3,740 scan load, 32 M bits
  - FP: 925 FFs, 1,320 scan load, 1.2 M bits

- Tester scan memory (optional)
  - 4G bits minimum
Outline

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CRC Tasks

- Architecture
- Detailed design, simulation
- Synthesis, timing closure
- Test sets generation
- Test program
- Package tests
- Test results analysis

LSI Tasks

- Synthesis, timing closure Support
- Layout
- Fabrication
- Wafer sort
- Packaging
- Probe card, load board

Functional Tests
