AN EXPERIMENTAL CHIP TO EVALUATE TEST TECHNIQUES
CHIP AND EXPERIMENT DESIGN

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PURPOSE

- Basic Problem
  100% Fault Coverage ➔ 0 DPM

- Objective
  - Thorough Experimental Comparison
  - Many Different Test Techniques
  - Escape Rate

PURPOSE

- Experimental Chip to Evaluate Test Techniques

Main Goals
- Real-World Circuits
- Evaluate Many Test Techniques
- Test Under Identical Conditions
- Include Exhaustive Tests as a Reference
- Real Production Failures, Not Injected Failures

Test Chip
- 25k Gates
- LSI Logic LFT150K CMOS Gate Array
- Over 5,491 Die Evaluated

OUTLINE

- Participants
- Previous Work
- Test Chip Architecture
- Test Plan
- Conclusion

PARTICIPANTS

- Hughes:
  - Architecture, Detailed Design, Simulation
- Stanford CRC:
  - Architecture, CUT Design, Test Sets, ATE Program, Analysis
- LSI Logic:
  - Layout, Fabrication, Package Prototypes
- Digital Testing Services:
  - ATE Program, Testing
- Others:
  - CrossCheck, Sandia, U. Iowa

RELATED WORK

- Direct Approach
  - Collect Field Failure Data
    - Difficult to Control, Sensitive Data
- Fault Injection
  - Injected Faults Representative?
- “Realistic” Fault Models
  - Multiple Stuck-At Faults, Inductive Fault Analysis
    - Does Benefit Outweigh Complexity?
- Statistical Models
  - Quality Level In Terms of Coverage and Yield
    - Validating Statistical Models?
PREVIOUS EXPERIMENTS

- Several Previous Experiments

<table>
<thead>
<tr>
<th>Chips</th>
<th>Tests</th>
</tr>
</thead>
<tbody>
<tr>
<td>Velazco 90</td>
<td>Design Verification</td>
</tr>
<tr>
<td>Elo 90</td>
<td>9 Boolean Tests</td>
</tr>
<tr>
<td>Das 90</td>
<td>78k Stuck-At</td>
</tr>
<tr>
<td>Pancolly 90, 92</td>
<td>970 Stuck-At, Various Delay, IDDQ</td>
</tr>
<tr>
<td>Maxwell 91, 92</td>
<td>16-26k Scan, Des. Ver., IDDQ</td>
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<tr>
<td>Perry 92</td>
<td>Many Stuck-At, IDDQ</td>
</tr>
<tr>
<td>Schiessler 93</td>
<td>1.4k Des. Ver., Scan, IDDQ</td>
</tr>
<tr>
<td>Gayle 93</td>
<td>10M Stuck-At, At-Speed, IDDQ</td>
</tr>
<tr>
<td>Wiscombe 93</td>
<td>10k Stuck-At, IDDQ</td>
</tr>
</tbody>
</table>

- Give Insights
- Compare Limited Number of Test Techniques

OUR APPROACH

- Specially Designed Test Chip
- More Thorough Experiment

- Many Testing Techniques Compared
- Exhaustive, $2^n$ Reference Tests
- Tested Different:
  - Design Styles
  - Clocking Methodologies and Speeds
  - Data Sources
  - Response Analysis
- Reasonable Sample Size
  - Over 5,491 Die
  - 20 CUTs Per Die

OUTLINE

- Participants
- Previous Work
- Test Chip Architecture
  - Block Diagram
  - Circuits Under Test
  - Test Application Modes
  - Response Evaluation
- Test Plan
- Conclusion

TEST CHIP ARCHITECTURE

- 3 Elements
  - Data Source
  - 5 Circuits-Under-Test (CUT) – 4 Copies Each
  - Separate Response Analysis

- 4 of CUTS
  - Response Analysis

CIRCUITS UNDER TEST

- Combinational
- 12 or 24 Inputs
- 5 Types of CUTs
  - Data Path Logic
    - Multiplier, Multiplier-Squarer
    - Manual Design
  - Control Logic
    - 3 DMA Read Buffer Control Implementations
    - Synthesized
- 4 Copies of Each CUT Type
CIRCUITS UNDER TEST

<table>
<thead>
<tr>
<th>Name</th>
<th>Inputs</th>
<th>Outputs</th>
<th>LSI Gates</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MUL</td>
<td>24</td>
<td>12</td>
<td>1,146</td>
<td>12x12 Multiplier</td>
</tr>
<tr>
<td>SQR</td>
<td>12</td>
<td>6</td>
<td>446</td>
<td>6x6 Multiplier Followed by Squarer</td>
</tr>
<tr>
<td>STD</td>
<td>24</td>
<td>12</td>
<td>298</td>
<td>Any LSI Gates</td>
</tr>
<tr>
<td>ELM</td>
<td>24</td>
<td>12</td>
<td>380</td>
<td>Elementary Gates</td>
</tr>
<tr>
<td>ROB</td>
<td>24</td>
<td>12</td>
<td>898</td>
<td>Robust Path-Delay Fault Testable</td>
</tr>
</tbody>
</table>

*1 LSI Gate is Approximately 4 Transistors

DATA SOURCES

- External Parallel Vectors
  - Direct
    - Design Verification, Stuck-At, Weighted Random, IDDQ
  - 2-Pattern
    - Delay Fault Tests
    - Simulate Scan
- Simulated Scan
  - Logic to Simulate 1 Bit Shift
- Internal Pseudo-Random/Exhaustive Vectors
  - Super-Exhaustive \(2^n\) for SQR CUT

CONTROL LOGIC BLOCK

- Three Implementations of the Same Function, Same Speed
  - Original Design
    - DMA Read Buffer Controller
    - 34 Inputs
  - Unconstrained Synthesis
    - 2-Level Minimization
    - Constrained Technology Mapping
  - Constrained Technology Mapping
    - 2-Level to 3-Level Robust
    - Unconstrained Technology Mapping

CLOCKING MODES

- Direct
  - "Conventional"
- Pulse Width
  - For Slow ATE
- Internally Generated
  - Tracks Process

RESPONSE EVALUATION – OUTPUT SAMPLING

- Four CUT Copies Compared

STABILITY CHECKING

- Technique for Delay Fault Testing [Franco 91]
  - First Experimental Evaluation
  - 216 Stability Checkers per Die
  - If (Change in Signal) AND (Checking Period=1) \(\Rightarrow\) ERROR=1
RESPONSE EVALUATION – STABILITY CHECKING

- All Stability Failures Detected
- No Comparators Needed

<table>
<thead>
<tr>
<th>CUT</th>
<th>Stability Checking</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copy 1</td>
<td>12</td>
</tr>
<tr>
<td>Copy 2</td>
<td>12</td>
</tr>
<tr>
<td>Copy 3</td>
<td>12</td>
</tr>
<tr>
<td>Copy 4</td>
<td>12</td>
</tr>
</tbody>
</table>

Stability Checking Error

FAILURE COUNTERS

- On-Chip Counters
  - First Sampling Error (24 Bits)
    - Sampling
    - Stability Checking
  - Total Number of Errors (16 Bits)
    - Sampling
    - Stability Checking
    - Stability Checking Only
- On-Chip Data Loggers
  - Scan Out at End of Test

SIGNATURE ANALYSIS

- Only on MUL CUT Type
- Area Overhead
- Both Serial and Parallel
  - Configurable
    - 12, 16, 24, 48 Bits
- Partial Evaluation Now
  - Too Much Test Time
  - MUX to Reconfigure and Share Logic
- More Thorough Evaluation On Interesting Dice Later
  - Reprobe or Packaged

OUTLINE

- Participants
- Previous Work
- Test Chip Architecture
  - Test Plan
    - Testing Strategy
    - Support Circuitry Tests
    - CUT Test Overview
- Conclusion

TESTING STRATEGY

- 2 Stage Testing

<table>
<thead>
<tr>
<th>Stage 1</th>
<th>Stage 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Wafer</td>
<td>CUT Test 1</td>
</tr>
<tr>
<td>5,491 Dice</td>
<td>CUT Test 2</td>
</tr>
<tr>
<td>5,491 Dice</td>
<td>...</td>
</tr>
<tr>
<td>5,491 Dice</td>
<td>CUT Test n</td>
</tr>
<tr>
<td>Confidential</td>
<td>Public</td>
</tr>
</tbody>
</table>

- Failures Targeted
  - “Hard-To-Detect” Defects, Not Gross Defects

SUPPORT CIRCUITRY TESTS

- Important To Have Thorough Tests
- 11 Scan Chains to Improve Testability
- Two Stuck-at Test Sets (98.8% Coverage)
- IDDQ Test with 250 Strobes
- Conservative Timing (Large Slack)
- CUT Inputs Held Constant
  - IDDQ Tests
  - CrossCheck Test Circuitry Tests
- No Evidence of Support Circuitry Failures in Stage 2 Testing
CUT TEST SETS

- Design Verification (Functional)
- ATPG:
  - Stuck-at, Stuck Open, Transition, Delay
  - Pin, Gate, Switch Level
  - Various Vendors, Coverages
- Pseudo-Random, Exhaustive, Super-Exhaustive
- Weighted Pseudo-Random
- CrossCheck
- IDDQ

TEST APPLICATION MODES

Data Source Modes
- Parallel
  - 1-Pattern
- Parallel
  - 2-Pattern
- Simulated
- Scan
- Internal
- Pseudorandom

Clocking Modes
- Direct
  - (At-Speed)
- Pulse Width
- Generated
- Internally
- Generated

Timing
- Rated
- Fast
- Slow

TEST APPLICATION

- Most Previous Tests
  - Repeated at Very-Low-Voltage [Hao 93]
  - 1.7 Volts
- Test Ordering
  - Exhaustive Test Repeated
    - Start of Test
    - End of Test
  - Consistency Check
    - Warming, Breaking During Tests

TEST ANALYSIS AND EVALUATION

- Test Chip Architecture Allows
  - On-Chip Data Collection for All Tests
  - Recorded on ATE After Each Test
- For Sampling and Stability Checking
  - First Fail Vector
  - Number of Failures
- Much More Data than Go/No Go for Each Test
  - Enables More Thorough Comparison of Test Techniques

CONCLUSION

- Described Experiment to Evaluate Test Techniques
  - Designed, Manufactured and Tested 5,491 Die
  - Evaluated Many Test Techniques
  - Real Production Failures
- Non-Trivial to Design and Perform Experiment
  - Defining the Architecture
  - Choice of CUTS
  - Large ATE Program
- Entire Design is Available
  - Can Do Similar Experiments in Other Technologies
- Results
  - Discussed in Next Presentation

EPILOGUE

- Test Chip Nickname
  - Murphy Chip
- Milestones
  - Nov 91 – First Hughes/Stanford Meeting
  - Jan 92 – Projected Completion Date – Dec 92
  - Feb 92 – 5 Sec. ATE Time, 20% Support Circuitry
  - Jun 92 – Finalized CUTs
  - Jul 93 – Started Testing Prototypes
  - Jun 94 – Started Production Testing
  - Jun 94 – 76 Sec. ATE Time, 50% Support Circuitry
  - Feb 95– Completed Production Testing
  - Oct 95 – Still Analyzing Data
PREVIOUS WORK

<table>
<thead>
<tr>
<th>Experiment</th>
<th>CUT</th>
<th>Test Applied</th>
<th>Results</th>
</tr>
</thead>
<tbody>
<tr>
<td>Velazco 90</td>
<td>900</td>
<td>Various les, Vrf. physically cut lines</td>
<td>Shorter tests have lower coverage</td>
</tr>
<tr>
<td>[Grenoble 90]</td>
<td>900</td>
<td>2,500 gate, 130,000 ICs</td>
<td>Various les, Vrf. physically cut lines</td>
</tr>
<tr>
<td>[Das 90]</td>
<td>900</td>
<td>7750 transistor, 77,912 ICs</td>
<td>99.7% Stuck-At coverage</td>
</tr>
<tr>
<td>[P document 90]</td>
<td>900</td>
<td>8,590 gate, 45,500 ICs</td>
<td>50% inductors, 90% inductors</td>
</tr>
<tr>
<td>[Maxwell 91]</td>
<td>900</td>
<td>8,590 gate, 26,550 ICs</td>
<td>Need all types of IDDQ tests for more defects</td>
</tr>
<tr>
<td>[Ando 91]</td>
<td>900</td>
<td>40K, 3M OSE, 400 ICs, 114, SOG</td>
<td>Need more testing for more defects</td>
</tr>
<tr>
<td>[Perry 92]</td>
<td>900</td>
<td>4,500 gate, 1 year of operation</td>
<td>99.9% Stuck-At</td>
</tr>
</tbody>
</table>

• Give Useful Insights, But Not Complete

POSSIBLE CRITICISMS

• Sample Size Too Small
  • Prototypes + 5,491 die, 20 CUTs/die
• Support Circuitry Tests Incomplete
  • Found No Problems With Support Circuitry in Stage 2 Tests
• Scaling of Results
  • Are results General, Scaling, What Predictions can be Made?
• Type I Errors
• Effect of Compaction of Responses on Test Analysis

EXPERIMENTAL RESULTS -- PROPAGATION DELAY

TEST CHIP EXPERIMENT

- Clock Rate At Which CUT Fails
- Average Data From 10 Working CUTs
- Slumberger 100MHz Tester
- Decrease Cycle In 25 ps Steps

<table>
<thead>
<tr>
<th>Cycle Time</th>
<th>Percent Faster</th>
</tr>
</thead>
<tbody>
<tr>
<td>10.295 ns</td>
<td>0.00%</td>
</tr>
<tr>
<td>10.245 ns</td>
<td>5.00%</td>
</tr>
<tr>
<td>10.240 ns</td>
<td>5.19%</td>
</tr>
<tr>
<td>10.235 ns</td>
<td>5.26%</td>
</tr>
<tr>
<td>10.230 ns</td>
<td>5.33%</td>
</tr>
<tr>
<td>10.225 ns</td>
<td>5.40%</td>
</tr>
<tr>
<td>10.220 ns</td>
<td>5.47%</td>
</tr>
<tr>
<td>10.215 ns</td>
<td>5.53%</td>
</tr>
<tr>
<td>10.210 ns</td>
<td>5.60%</td>
</tr>
<tr>
<td>10.205 ns</td>
<td>5.67%</td>
</tr>
</tbody>
</table>

Period = 10.295 ns (97 MHz)