AN EXPERIMENTAL CHIP TO EVALUATE TEST TECHNIQUES
EXPERIMENT RESULTS

Siyad Ma, Piero Franco, Edward J. McCluskey
Center for Reliable Computing
Stanford University
Stanford, CA 94305

Outline
• Test Strategy
• CUT Test Sets
• Test Conditions
• Results
• Summary

Test Strategy

Circuits Under Test

5 CUT Designs, 4 Copies Each
• SQR 6x6 Multiplier Plus Squarer
• MUL 12x12 Multiplier
• STD RB - Standard Gates
• ELM RB - Elementary Gates
• ROB RB - Robustly Delay Fault Testable

Test Pattern Contributors

• CAD Vendors
• Universities

Thanks to All Contributors!
### CUT Test Sets
- Design Verification
- Single Stuck-at
- Switch-Level
- Pseudo-Random
- Super-Exhaustive
- Weighted Random
- Osc. & Delay Line

### Single Stuck-At Tests
- Stuck Open
- Transition
- Gate Delay
- Path Delay
- CrossCheck
- Signature
- IDDQ

### Outline
- Test Strategy
- CUT Test Sets
- Test Conditions
- Results
- Summary

### Test Conditions
- 2 Application Modes
  - Parallel Load
  - Simulated Scan
- 3 Clocking Modes
  - Direct from ATE
  - Pulse Width Generated
  - Internally Generated

### Test Conditions
- 3 Clocking Speeds
  - Rated
  - Slow (2/3 Rated)
  - Fast (5-25% Faster than Rated)
- 2 Supply Voltages
  - Normal Voltage (5V)
  - Very-Low-Voltage (1.7V)
  - Speed: 5.6x Slower than Rated
  - No Exhaustive Tests

### Test Conditions
- 4 Different ATPG Tools
  - 80-100% Fault Coverage
  - 5 Detects, 15 Detects
  - Pin Faults
  - Compressed
An Experimental Chip to Evaluate Test Techniques-Experiment Results

**Results**

- 4 wafer lots
- Detected by:
  - Sampling @ Normal Voltage
  - Sampling @ Very-Low-Voltage
  - CrossCheck
  - IDDQ

Yield = 97.04%

**Sampling @ Normal Voltage**

<table>
<thead>
<tr>
<th>CUT Type</th>
<th>Gate Count</th>
<th>Fail All Tests</th>
<th>Fail Some Tests</th>
</tr>
</thead>
<tbody>
<tr>
<td>SQR</td>
<td>1784</td>
<td>19</td>
<td>2</td>
</tr>
<tr>
<td>MUL</td>
<td>4584</td>
<td>40</td>
<td>15</td>
</tr>
<tr>
<td>STD</td>
<td>1520</td>
<td>17</td>
<td>5</td>
</tr>
<tr>
<td>ELM</td>
<td>1192</td>
<td>16</td>
<td>7</td>
</tr>
<tr>
<td>ROB</td>
<td>3992</td>
<td>35</td>
<td>21</td>
</tr>
<tr>
<td>Total</td>
<td>12672</td>
<td>127</td>
<td>50</td>
</tr>
</tbody>
</table>

**Stuck-At Test Escapes**

- Yet to Be Analyzed
  - Stability Checking
  - Simulated Scan
  - Signature Analysis
  - Other Clocking Modes
  - Failure Counters

**Pseudo-Random vs. Single Stuck-At ATPG**

- Test Set Limits
  - Minimum Fault Coverage
  - Maximum Test Length

- For Same Fault Coverage
  - Fewer Escapes for Pseudo-Random

- For Same Test Length
  - Fewer Escapes for Stuck-At ATPG
An Experimental Chip to Evaluate Test Techniques-Experiment Results

**Sampling @ Normal Voltage**
- **Design Verification**
  - Poor Coverage:
    - 7 Escapes in 15 Interesting MUL CUTs
- **Single Stuck-At Tests**
  - Escapes at 100% Stuck-At Coverage

**Sampling @ Normal Voltage**
- **Pseudo-Random**
  - CUT Escape at 100K Vectors
- **Weighted Random**
  - For Equivalent Test Lengths
    - Multiple Weights ⇒ Fewer Escapes

**Test Escapes @ Slow Speed**

<table>
<thead>
<tr>
<th>CUTs</th>
<th>Rated Speed</th>
<th>Slow Speed (2/3 Rated Speed)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ELM #63</td>
<td>Fail Some Tests</td>
<td>Pass All Tests</td>
</tr>
<tr>
<td>ROB #93</td>
<td></td>
<td></td>
</tr>
<tr>
<td>STD #79</td>
<td>Pass 100% Pin only</td>
<td>Fail Exhaustive and Path Delay</td>
</tr>
<tr>
<td>ROB #96</td>
<td>Pass Some Tests</td>
<td>Pass 100% Pin, Gate Delay + Tests Passed at Rated Speed</td>
</tr>
</tbody>
</table>

**Very-Low-Voltage Test**

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Normal Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pass</td>
<td>5353 dice</td>
</tr>
<tr>
<td>Fail</td>
<td>13 dice</td>
</tr>
</tbody>
</table>

* No exhaustive tests

**Test Results**

- **Sampling @ Normal Voltage**
- **Sampling @ Very-Low-Voltage**
- **CrossCheck**
- **IDDQ**

- **Very-Low-Voltage Test**
  - Normal Voltage
    - Pass
    - Fail
    - Pass 5353 dice
    - Fail 13 dice

* No exhaustive tests
An Experimental Chip to Evaluate Test Techniques-Experiment Results

CrossCheck Tests

<table>
<thead>
<tr>
<th>Normal Voltage</th>
<th>Pass</th>
<th>Fail</th>
</tr>
</thead>
<tbody>
<tr>
<td>CrossCheck Pass</td>
<td>5366 dice</td>
<td>3 dice*</td>
</tr>
<tr>
<td>CrossCheck Fail</td>
<td>0 dice</td>
<td>122 dice</td>
</tr>
</tbody>
</table>

* Also speed dependent

Test Results

- Sampling @ Normal Voltage
- Sampling @ Very-Low-Voltage
- CrossCheck
  - IDDQ

Test Results

- Sampling @ Normal Voltage
- Sampling @ Very-Low-Voltage
- CrossCheck
  - IDDQ

IDDQ Measurements

- At 200μA threshold
- 36 IDDQ escapes, 15 IDDQ only

IDDQ Test Length

- ATPG 1 = 19
- ATPG 2 = 90
- PR = 64
- Total # Defective MUL=40

Preliminary Results

- Stability Checking
  - 21 MUL CUT failures
    - Failed sampling tests
    - 16 speed dependent failures
    - 3 Very-Low-Voltage only failures

Outline

- Test Strategy
- Test Sets
- Test Conditions
- Results
  - Summary
An Experimental Chip to Evaluate Test Techniques-Experiment Results

Summary

**All Wafers Tested**
- Stage 2 Test Data Complete
- Large Amount of Data for Each Failing Die
- Analysis Still in Progress
  - Stability Checking
  - Signature Analysis
  - Other Clocking Modes
  - Simulated Scan
  - Failure Counters

**Normal Voltage, Rated Speed**
- Stuck-At ATPG
  - Test Escapes at 100% Fault Coverage
- Pseudo-Random
  - Test Escapes at 99% Fault Coverage

**Slow Speed**
- 4 Speed Dependent Failures

**Very-Low-Voltage**
- Some VLV Only Failures
  - Potential Weak Parts
  - Need Further Tests

**IDDQ**
- Must Be Used With Voltage Tests
- Some IDDQ Only
  - Potential Weak Parts
  - Efficiency: Varies From Tool to Tool

**Future Plans**

**Reprobe**
- Repeat Tests
- Other Tests

**Early Life Failure Test**
- Run 1 Year on Packaged Parts

**Burn-In**

**Failure Analysis**